LTC2933:
Safety Application Note

Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

SEPTEMBER 2025

Contents

1 | Overview

The scope of this document is to provide information to support integrating the LTC2933 into functional safety designs. This contains:

- Failure-In-Time (FIT) of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

General Description

The LTC2933 is an EEPROM configurable voltage supervisor which can simultaneously monitor up to six power supply voltage inputs. Each voltage detector offers I^2C programmable over/undervoltage thresholds in various ranges and increments.

Two general purpose inputs (GPI) can be configured as programmable manual reset ($\overline{MR}$), UV disable ($\overline{UVDIS}$), margin ($\overline{MARG}$) or auxiliary comparator (AUXC) inputs. Three general purpose pins (GPIO) can be configured for input or output operation. When configured as an input, a GPIO pin can be mapped to any other GPIO configured as an output. The GPIO pins can also be configured as ALERT or fault outputs. Faults can be configured with programmable delay-on-release times. Output type and polarity are also configurable.

Status and history registers log faults and can be polled via the I^2C interface. A fault snapshot is also backed up in internal EEPROM. All parameters are programmable via the I^2C interface. Configuration EEPROM supports autonomous operation without additional software.

Table 1-1 below shows the product description with an example application configuration wherein GPIO1 and GPIO2 are configured as open-drain, active-low outputs, while GPIO3 is configured as active-high output.

Table 1-1 Product Description

Part Number	Primary Function	System Function
LTC2933	Programmable Hex Voltage Supervisor with EEPROM	Monitor if a power supply is above the OV threshold or below the UV threshold and assert GPIO1, GPIO2 output signals LOW and GPIO3 output signal HIGH.

Figure 1-1 shows the product-specific block diagram of the LTC2933.

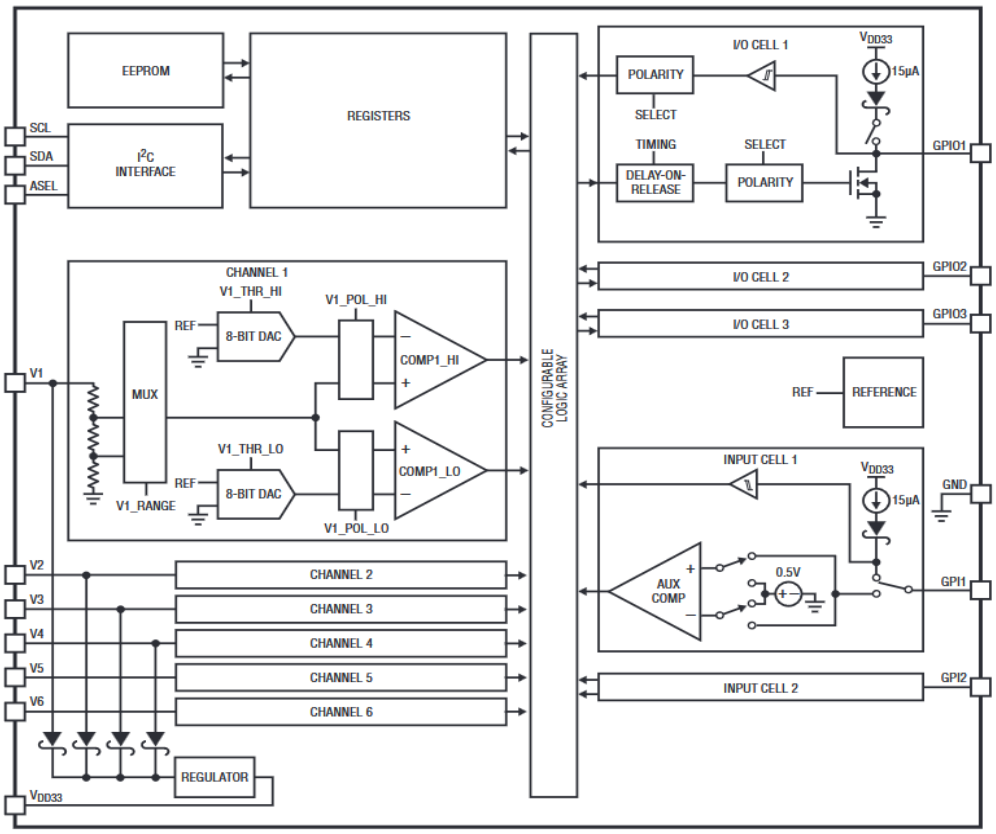

Figure 1-1 LTC2933 Functional Block Diagram

The LTC2933 was developed following a quality-managed development process in compliance with the ISO 9001 quality management system standard but was not developed in compliance with the IEC61508 safety standard. The associated certificates are available on Quality Certificates | Analog Devices.

2 | Functional Safety Failure-In-Time (FIT)

This section offers specific details on the base functional safety failure-in-time (FIT) for the LTC2933, according to SN 29500, IEC 62380 and accelerated testing conditions of HTOL. It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- Table 2-1 provides FIT according to SN 29500
- Table 2-2 provides FIT according to IEC 62380
- Table 2-3 provides FIT according to HTOL

The FIT of the LTC2933 based on SN 29500 for a specific industrial mission profile is detailed below:

Table 2-1 Functional Safety Component FIT According to SN 29500

SN 29500 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Predicted Component FIT	85.28

- Mission Profile: 20 years constant operation at 55°C temperature
- Operating Voltage (max): 13.9V (based on product datasheet)
- Power Dissipation: 20mW
- Theta-JA: 110 °C/W

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on SN 29500.

- SN 29500 part: Part 2 Table 5 under ASICs
- Sub-category: CMOS, BiCMOS
- Integration Density: 5k-50k
- Part is sensitive to drift

The FIT of the LTC2933 based on IEC 62380 for a specific industrial mission profile is detailed below:

Table 2-2 Functional Safety Component FIT According to IEC 62380

IEC 62380 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Total Component FIT	37.69
Die FIT	37.11
Package FIT	0.58

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on IEC 62380.

- FIT calculation model: Section 7.3.1, refer to Mathematical Model
- IEC 62380 part and section for die FIT: Table 16, MOS ASIC circuits, Full Custom
- Production year: 2017
- Integration Density: 5k-50k
- Climate type: World-wide (Table 8)
- IEC 62380 part and section for package FIT: Table 17b, Two Rows Connection Packages
- Package type: SSOP 16 pins, length: 4.89mm, width: 3.89mm, pitch: 0.64mm
- Technology Structure: MOS BiCMOS (Low Voltage)
- Substrate Material: Epoxy Glass (FR4, G-10)
- EOS FIT rate assumed: 0 FIT

The FIT of the LTC2933 based on accelerated testing conditions of HTOL is detailed below:

Table 2-3 Functional Safety Component FIT According to HTOL Testing

Confidence Level	FIT (Failures Per 10^9 Hours)
70%	0.12
90%	0.23
95%	0.30
99%	0.46

Note 3: The FIT for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 56686
- Number of Failures: 0
- Activation Energy: 0.7eV
- Accelerated Temperature: 55degC
- Equivalent Accelerated Device Hours: 10,078,622,220

3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

Two (2) application circuits, Application Circuit 1 and Application Circuit 2, were considered in calculating the FMD. The failure mode distribution estimation tables for the LTC2933 are derived from the component die area ratio and complexity, and from engineering expertise.

3-1 Application Circuit 1

In this application, the LTC2933 is monitoring six (6) voltage rails that are supplied into a system. The general-purpose inputs/outputs GPIO1 and GPIO2 are configured as active-LOW, open-drain outputs pulled to an external voltage VPULLUP, through a pull-up resistor. GPIO3, on the other hand, is configured to be an active-high output with a weak pull-down resistor to GND. The general-purpose inputs, GPI1 and GPI2, are configured as active-LOW manual resets, thus pulling these pins low will force GPIO1 and GPIO2 output pins to low and GPIO3 output pin to high.

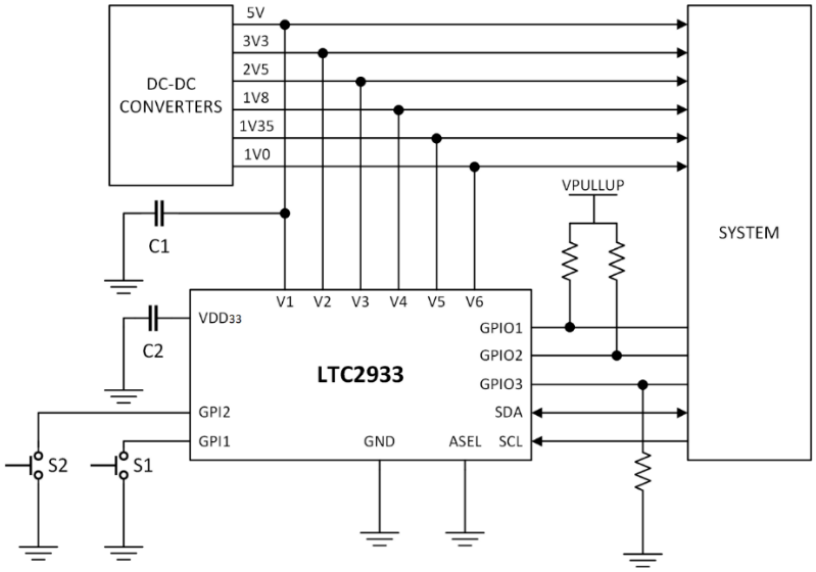

Figure 3-1 Application Circuit 1 Simplified Schematic Diagram

System Function

- Monitor if a power supply is above the OV threshold or below the UV threshold and assert GPIO1, GPIO2 output signals LOW and GPIO3 output signal HIGH.

Table 3-1 Failure Mode Distribution

Failure Modes	Failure Mode Distribution
At least one of the GPIO indicates a trip when it should not	45%
At least one of the GPIO doesn't indicate a trip when it should	50%
No effect in SF1	5%

3-2 Application Circuit 2

In this application, the LTC2933 is monitoring four (4) voltage rails that are supplied into a system. The unused channels, V5 and V6 are connected to ground (GND). The general-purpose inputs/outputs pins GPIO1 and GPIO2 are configured as active-LOW, open-drain outputs pulled to an external voltage VPULLUP, through a pull-up resistor. On the other hand, GPIO3 is configured to be an active-high output with a weak pull-down resistor to GND. The general-purpose inputs, GPI1 and GPI2, are configured as active-LOW manual resets, thus pulling these pins low will force GPIO1 and GPIO2 output pins to low and GPIO3 output pin to high.

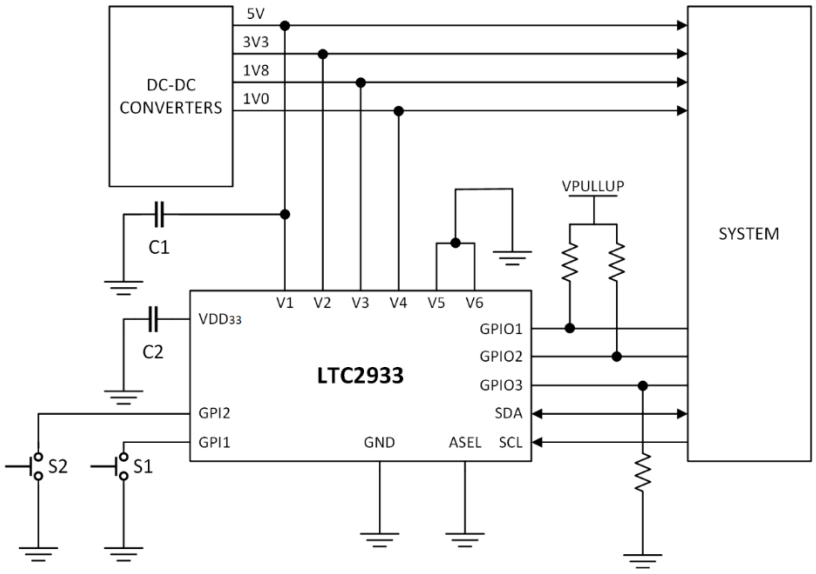

Figure 3-2 Application Use Case 2 Simplified Schematic Diagram

System Function

- Monitor if a power supply is above the OV threshold or below the UV threshold and assert GPIO1, GPIO2 output signals LOW and GPIO3 output signal HIGH.

Table 3-2 Failure Mode Distribution

Failure Modes	Failure Mode Distribution
At least one of the GPIO indicates a trip when it should not	44%
At least one of the GPIO doesn't indicate a trip when it should	50%
No effect in SF1	6%

4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for the LTC2933. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see Table 4-1 and Table 4-2)
- Pin short-circuited to GND (see Table 4-3 and Table 4-4)
- Pin open-circuited (see Table 4-5 and Table 4-6)
- Pin short-circuited to adjacent pins (see Table 4-7 and Table 4-8)

Figure 4-1 illustrates the pin diagram for the LTC2933, particularly the SSOP package. Refer to the product datasheet for a detailed description of each pin's function.

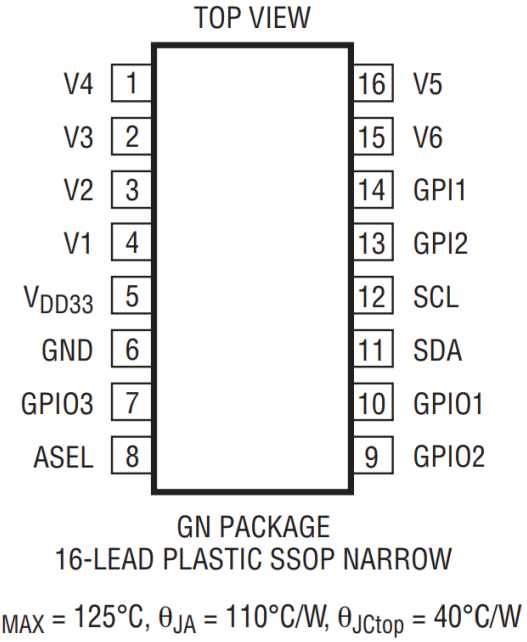

Figure 4-1. LTC2933 Pin Diagram

Below are the usage assumptions and device configuration considered for the Pin FMEA:

- The GPIO output pins were configured as per application circuits 1 and 2. See discussions on sections 3-1 and 3-2.
- The monitoring pins are configured as per applications circuits on Figures 3-1 and 3-2.
- The supply voltage range (Vn) is from 3.4V to 13.9V for V1 and 3.4V to 5.8V for V2 to V4, and the operating temperature range (T_A) is from - 40°C to +85°C.

Table 4-1 Application Circuit 1 Pin FMEA for the LTC2933 Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	V4	OV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
2	V3	OV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
3	V2	OV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
4	V1	No effect. V1 is the chip supply.
5	VDD33	Internal regulator shorted to supply. Part damaged.
6	GND	Part not functional.
7	GPIO3	GPIO3 always HIGH.
8	ASEL	Part will not respond to I2C but can still monitor voltages. No effect to supply monitoring.
9	GPIO2	Only GPIO2 always HIGH.
10	GPIO1	Only GPIO1 always HIGH.
11	SDA	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
12	SCL	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
13	GPI2	Manual reset will not be detected. No effect in supply monitoring.
14	GPI1	Manual reset will not be detected. No effect in supply monitoring.
15	V6	OV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
16	V5	OV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.

Table 4-2 Application Circuit 2 Pin FMEA for the LTC2933 Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	V4	OV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
2	V3	OV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
3	V2	OV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
4	V1	No effect. V1 is the chip supply.
5	VDD33	Internal regulator shorted to supply. Part damaged.
6	GND	Part not functional.
7	GPIO3	GPIO3 always HIGH.
8	ASEL	Part will not respond to I2C but can still monitor voltages. No effect to supply monitoring,
9	GPIO2	Only GPIO2 always HIGH.
10	GPIO1	Only GPIO1 always HIGH.
11	SDA	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
12	SCL	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
13	GPI2	Manual reset will not be detected. No effect in supply monitoring.
14	GPI1	Manual reset will not be detected. No effect in supply monitoring.
15	V6	Part not functional.
16	V5	Part not functional.

Table 4-3 Application Circuit 1 Pin FMEA for the LTC2933 Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	V4	UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
2	V3	UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
3	V2	UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
4	V1	No power for internal circuit. Part not functional.
5	VDD33	Internal regulator shorted to ground. Part not functional.
6	GND	No effect. Pin is GND.
7	GPIO3	GPIO3 always LOW.
8	ASEL	No effect. Pin is connected to GND.
9	GPIO2	Only GPIO2 always LOW.
10	GPIO1	Only GPIO1 always LOW.
11	SDA	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
12	SCL	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
13	GPI2	Forced reset. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
14	GPI1	Forced reset. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
15	V6	UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
16	V5	UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.

Table 4-4 Application Circuit 2 Pin FMEA for the LTC2933 Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	V4	UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
2	V3	UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
3	V2	UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
4	V1	No power for internal circuit. Part not functional.
5	VDD33	Internal regulator shorted to ground. Part not functional.
6	GND	No effect. Pin is GND.
7	GPIO3	GPIO3 always LOW.
8	ASEL	No effect. Pin is connected to GND.
9	GPIO2	Only GPIO2 always LOW.
10	GPIO1	Only GPIO1 always LOW.
11	SDA	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
12	SCL	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
13	GPI2	Forced reset. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
14	GPI1	Forced reset. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
15	V6	No effect. Connected to GND since input is not monitored.
16	V5	No effect. Connected to GND since input is not monitored.

Table 4-5 Application Circuit 1 Pin FMEA for the LTC2933 Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	V4	Internal UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
2	V3	Internal UV. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
3	V2	Internal UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
4	V1	IC supply. No power for internal circuit. Part not functional.
5	VDD33	Damage to internal circuit. Part not functional.
6	GND	Part not functional.
7	GPIO3	GPIO3 pin unconnected to external pull-down. Can't pull HIGH. Always LOW.
8	ASEL	Part will not respond to I2C but can still monitor voltages. No effect to supply monitoring,
9	GPIO2	GPIO2 pin unconnected to external pull-up. Can't pull LOW. Always HIGH.
10	GPIO1	GPIO1 pin unconnected to external pull-up. Can't pull LOW. Always HIGH.
11	SDA	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
12	SCL	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
13	GPI2	Manual reset will not be detected. No effect in supply monitoring.
14	GPI1	Manual reset will not be detected. No effect in supply monitoring.
15	V6	Internal UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
16	V5	Internal UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.

Table 4-6 Application Circuit 2 Pin FMEA for the LTC2933 Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	V4	Internal UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
2	V3	Internal UV. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
3	V2	Internal UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
4	V1	IC supply. No power for internal circuit. Part not functional.
5	VDD33	Damage to internal circuit. Part not functional.
6	GND	Part not functional.
7	GPIO3	GPIO3 pin unconnected to external pull-down. Can't pull HIGH. Always LOW.
8	ASEL	Part will not respond to I2C but can still monitor voltages. No effect to supply monitoring,
9	GPIO2	GPIO2 pin unconnected to external pull-up. Can't pull LOW. Always HIGH.
10	GPIO1	GPIO1 pin unconnected to external pull-up. Can't pull LOW. Always HIGH.
11	SDA	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
12	SCL	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
13	GPI2	Manual reset will not be detected. No effect in supply monitoring.
14	GPI1	Manual reset will not be detected. No effect in supply monitoring.
15	V6	No effect. Connected to GND since input is not monitored.
16	V5	No effect. Connected to GND since input is not monitored.

Table 4-7 Application Circuit 1 Pin FMEA for the LTC2933 Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	V4	V3	Inputs shorted together. OV/UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
2	V3	V2	Inputs shorted together. OV/UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
3	V2	V1	Inputs shorted together. OV/UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
4	V1	VDD33	Internal regulator shorted to supply. Part damaged.
5	VDD33	GND	Internal regulator shorted to ground. Part not functional.
6	GND	GPIO3	Only GPIO3 always LOW.
7	GPIO3	ASEL	GPIO3 always LOW.
8	ASEL	GPIO2	Only GPIO2 always LOW.
9	GPIO2	GPIO1	Outputs shorted together. GPIO1 and GPIO2 OR-ed together. No effect to supply monitoring.
10	GPIO1	SDA	GPIO1 may trigger I2C communication. No effect to supply monitoring.
11	SDA	SCL	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
12	SCL	GPI2	GPIO2 is triggered when SCL pulls LOW. No effect to supply monitoring,
13	GPI2	GPI1	Reset inputs shorted. Reset LOW in GPI2 will also trigger GPI1. No effect to supply monitoring.
14	GPI1	V6	Shorted to input. OV detected at V6. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
15	V6	V5	Inputs shorted together. OV/UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
16	V5	V4	Inputs shorted together. OV/UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.

Table 4-8 Application Circuit 2 Pin FMEA for the LTC2933 Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	V4	V3	Inputs shorted together. OV/UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
2	V3	V2	Inputs shorted together. OV/UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
3	V2	V1	Inputs shorted together. OV/UV detected. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.
4	V1	VDD33	Internal regulator shorted to supply. Part damaged.
5	VDD33	GND	Internal regulator shorted to ground. Part not functional.
6	GND	GPIO3	Only GPIO3 always LOW.
7	GPIO3	ASEL	GPIO3 always LOW.
8	ASEL	GPIO2	Only GPIO2 always LOW.
9	GPIO2	GPIO1	Outputs shorted together. GPIO1 and GPIO2 OR-ed together. No effect to supply monitoring.
10	GPIO1	SDA	GPIO1 may trigger I2C communication. No effect to supply monitoring.
11	SDA	SCL	Cannot configure device but part can still monitor voltages. No effect to supply monitoring.
12	SCL	GPI2	GPIO2 is triggered when SCL pulls LOW. No effect to supply monitoring,
13	GPI2	GPI1	Reset inputs shorted. Reset LOW in GPI2 will also trigger GPI1. No effect to supply monitoring.
14	GPI1	V6	Forced reset since V6 is connected to GND. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.

Table 4-8 Application Circuit 2 Pin FMEA for the LTC2933 Pins Short-Circuited to Adjacent Pins (Cont.)

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
15	V6	V5	No effect. Connected to GND since input is not monitored.
16	V5	V4	Inputs shorted together. UV detected at V4. Both GPIO1 and GPIO2 are always LOW. GPIO3 always HIGH.

5 | Revision History

Revision	Revision Date	Description
A	22Mar25	Initial Release
B	31Mar25	Corrected some minor grammatical errors.
C	03Apr25	Under Section 3-2, the table title was corrected from “3-1” to “3-2”. Added a period to end the second paragraph in the last page.
D	11Sep25	Updated the FMD section to remove correction factor. Corrected minor typographical errors.

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