

# LT8300: Safety Application Note

## Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

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### JANUARY 2026

#### Contents

1   Overview .....	2
2   Functional Safety Failure-In-Time (FIT).....	3
3   Failure Mode Distribution (FMD) .....	5
4   Pin Failure Mode and Effects Analysis (Pin FMEA) .....	6
5   Revision History .....	8

# 1 | Overview

The scope of this document is to provide information to support integrating the LT8300 into functional safety designs. This contains:

- Failure-In-Time (FIT) of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

## General Description

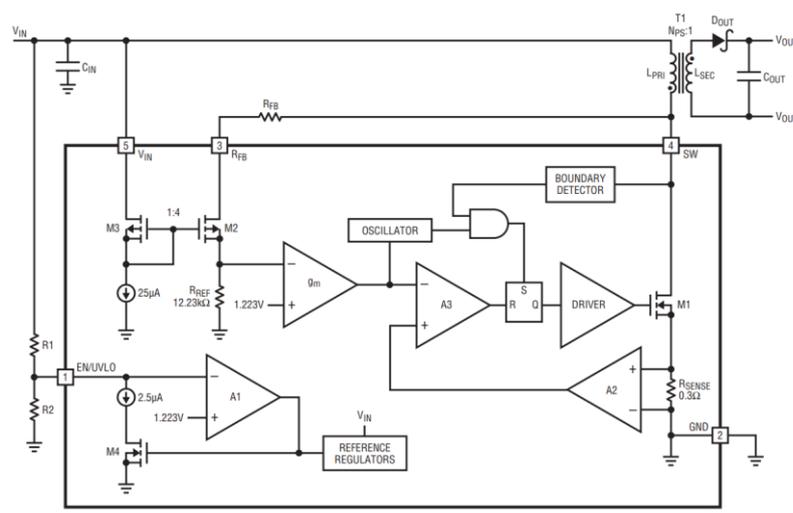
The LT8300 is a micropower high voltage isolated flyback converter. By sampling the isolated output voltage directly from the primary-side flyback waveform, the part requires no third winding or opto-isolator for regulation. The output voltage is programmed with a single external resistor. Internal compensation and soft-start further reduce external component count. Boundary mode operation provides a small magnetic solution with excellent load regulation. Low ripple Burst Mode operation maintains high efficiency at light load while minimizing the output voltage ripple. A 260mA, 150V DMOS power switch is integrated along with all high voltage circuitry and control logic into a 5-lead ThinSOT™ package.

The LT8300 operates from an input voltages range of 6V to 100V and can deliver up to 2W of isolated output power. The high level of integration and the use of boundary and low ripple burst modes result in a simple to use, low component count, and high efficiency application solution for isolated power delivery.

**Table 1-1 Product Description**

Part Number	Primary Function	System Function
LT8300	100VIN Micropower Isolated Flyback Converter with 150V/260mA Switch	Supply isolated power with regulated output voltage within tolerance.

Figure 1-1 shows the product specific block diagram of LT8300.



**Figure 1-1 LT8300 Block Diagram**

LT8300 was developed following a quality-managed development process in compliance with the ISO 9001 quality management system standards but was not developed in compliance with the IEC 61508 safety standard. The associated certificates are available on [Quality Certificates | Analog Devices](#).

## 2 | Functional Safety Failure-In-Time (FIT)

This section offers specific details on the base functional safety failure-in-time (FIT) for the LT8300, according to SN 29500, IEC 62380 and accelerated testing conditions of high-temperature operating life (HTOL). It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- [Table 2-1](#) provides FIT according to SN 29500
- [Table 2-2](#) provides FIT according to IEC 62380
- [Table 2-3](#) provides FIT according to HTOL

The FIT of LT8300 based on SN 29500 for a specific industrial mission profile is detailed below:

**Table 2-1 Functional Safety Component FIT According to SN 29500**

SN 29500 Industrial Mission Profile	FIT (Failures Per 10 <sup>9</sup> Hours)
Predicted Component FIT	95.81

- Mission Profile: 20 years constant operation at 55°C temperature
- Operating Voltage (max): 100V
- Power Dissipation: 0.189W (operating at 0.15A Load)
- Theta-JA: 150°C/W

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on SN 29500.

- SN 29500 part: Part 2 Table 5 under ASICs
- Sub-category: CMOS, BiCMOS
- Integration Density: 50-5k
- Part is sensitive to drift

The FIT of LT8300 based on IEC 62380 for a specific industrial mission profile is detailed below:

**Table 2-2 Functional Safety Component FIT According to IEC 62380**

IEC 62380 Industrial Mission Profile	FIT (Failures Per 10 <sup>9</sup> Hours)
Total Component FIT	13.07
Die FIT	12.96
Package FIT	0.11

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on IEC 62380.

- FIT calculation model: Section 7.3.1, refer to Mathematical Model
- IEC 62380 part and section for die FIT: Table 16, MOS ASIC circuits, Full Custom
- Production year: 2019
- Integration Density: 50-5k
- Climate type: World-wide (Table 8)
- IEC 62380 part and section for package FIT: Table 17b, Two rows Connection Packages
- Package type: TSOT 5 pins, length: 2.8mm, width: 1.625mm, pitch: 0.95mm
- Technology Structure: MOS BiCMOS (High Voltage)
- Substrate Material: Epoxy Glass (FR4, G-10)
- EOS FIT assumed: 0 FIT

The FIT of LT8300 based on accelerated testing conditions of HTOL is detailed below:

**Table 2-3 Functional Safety Component FIT According to HTOL Testing**

<b>Confidence Level</b>	<b>FIT (Failures Per 10<sup>9</sup> Hours)</b>
70%	0.17
90%	0.33
95%	0.44
99%	0.67

Note 3: The FIT values for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 38,151
- Number of Failures: 0
- Activation Energy: 0.7eV
- Accelerated Temperature: 55°C
- Equivalent Accelerated Device Hours: 6,879,916,434

### 3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

Table 3-1 shows the failure mode distribution estimation for LT8300 as derived from the component die area ratio and complexity, and from engineering expertise.

#### Application Circuit

In this application, the power supply connected to the VIN pin operates at 24V. The output operates at 5V with full load current of 0.15A. EN/UVLO pin is connected to VIN via a resistor divider with 7V set as UVLO and 1V as hysteresis. Other pins such as RFB and SW are configured as shown in Figure 3-1.

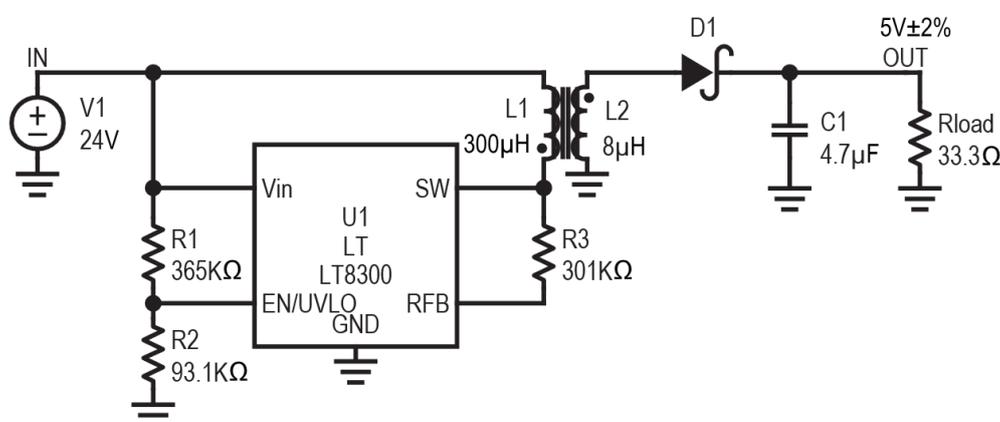


Figure 3-1 LT8300 Typical Application Circuit

#### System Function

- Supply isolated power with regulated output voltage (VOUT) within tolerance.

Table 3-1 Failure Mode Distribution

System Failure Modes	Failure Mode Distribution
VOUT is 0V.	49%
VOUT is above target regulation (>+2%). <sup>1</sup>	8%
VOUT is below target regulation (<-2%). <sup>2</sup>	8%
VOUT is oscillating beyond regulation tolerance. <sup>3</sup>	18%
No effect. <sup>4</sup>	17%

Note 4:

<sup>1</sup> 5.1V < VOUT < VIN

<sup>2</sup> 0V < VOUT < 4.9V

<sup>3</sup> Can involve one or more of the following:

- Part of VOUT oscillation either exceeds + 2% of target, or goes below - 2% of target, or violates both limits.
- VOUT is indeterminate due to intermittent or indeterminate switching on SW pin, and worst-case failure is assumed and binned under this failure mode.

<sup>4</sup> No effect or has increased/decreased operating switching frequency and/or quiescent current. Output oscillating but within +/- 2% of target.

Note 5: The system failure modes shown in Table 3-1 are ones which the IC failures will lead to.

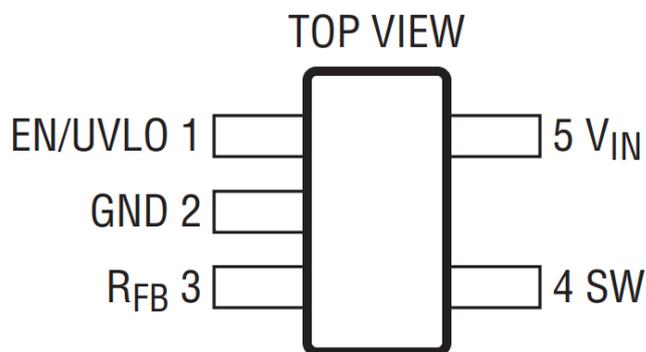
Note 6: Failures of external components are not covered in the analysis.

## 4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for LT8300. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see [Table 4-1](#))
- Pin short-circuited to GND (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to adjacent pins (see [Table 4-4](#))

Figure 4-1 illustrates the pin diagram for LT8300. Refer to the product datasheet for a detailed description of each pin's function.



**Figure 4-1. LT8300 Pin Diagram**

Below are the usage assumptions and device configuration considered for the Pin FMEA:

- Pin connections were configured as per application circuit. See discussions on section 3.
- The operating voltage range ( $V_{IN}$ ) is from 6V to 100V, and the operating temperature range ( $T_A$ ) is from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

**Table 4-1 Pin FMEA for LT8300 Pins Short-Circuited to Supply**

Pin no.	Pin Name	Effect of Failure Mode
1	EN/UVLO	UVLO will not take effect. IC is still enabled. No effect on output voltage.
2	GND	No power for the IC. Output stays at 0V.
3	RFB	Output won't regulate.
4	SW	The flyback output stays at 0V.
5	VIN	No effect.

**Table 4-2 Pin FMEA for LT8300 Pins Short-Circuited to GND**

Pin no.	Pin Name	Effect of Failure Mode
1	EN/UVLO	IC is disabled. Output stays at 0V.
2	GND	No effect.
3	RFB	Abs max rating will be violated. Output is oscillating and below target regulation.
4	SW	No switching. Output stays at 0V.
5	VIN	No power for the IC. Output is 0V.

**Table 4-3 Pin FMEA for LT8300 Pins Open-Circuited**

Pin no.	Pin Name	Effect of Failure Mode
1	EN/UVLO	The flyback output stays at 0V.
2	GND	The flyback output stays at 0V.
3	RFB	Output won't regulate.
4	SW	The flyback output stays at 0V.
5	VIN	The flyback output stays at 0V.

**Table 4-4 Pin FMEA for LT8300 Pins Short-Circuited to Adjacent Pins**

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	EN/UVLO	VIN	UVLO will not take effect. IC is still enabled. No effect on output voltage.
2	GND	EN/UVLO	IC is disabled. Output stays at 0V.
3	RFB	GND	Abs max rating will be violated. Output is oscillating and below target regulation.
4	SW	RFB	Abs max rating of RFB pin will be violated. Output stays at 0V.
5	VIN	SW	The flyback output stays at 0V.

## 5 | Revision History

Revision	Revision Date	Description
A	28Jan26	Initial Release

## IMPORTANT NOTES AND DISCLAIMER

PLEASE BE AWARE THAT THE PRODUCT IN QUESTION HAS NOT BEEN DEVELOPED IN ACCORDANCE WITH INDUSTRIAL SAFETY STANDARDS AND IS NOT RECOMMENDED FOR SUCH APPLICATIONS AS PER THE SPECIFIC DATA SHEET. THIS REPORT IS INTENDED SOLELY TO PROVIDE THE CUSTOMER WITH DETAILED INFORMATION ON FAILURE MODES AND THEIR DISTRIBUTION ACCORDING TO IEC61508, RELATED TO THE POTENTIAL USE OF QUALITY-MANAGED PARTS FOR SPECIFIC HARDWARE EVALUATION CLASS AS DESCRIBED IN THIS STANDARD.

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