ADP7156:
Safety Application Note

Failure-In-Time, Failure Mode Distribution and Pin Failure Mode and Effects Analysis

NOVEMBER 2025

Contents

1 | Overview

The scope of this document is to provide information to support integrating the ADP7156 into functional safety designs. This contains:

- Failure-In-Time (FIT) of the component calculated in accordance with the industry reliability standards
- Failure Mode Distribution of the device (FMD)
- Pin Failure Mode and Effects Analysis (Pin FMEA)

General Description

The ADP7156 is a linear regulator that operates from 2.3V to 5.5V and provides up to 1.2A of output current. Using an advanced proprietary architecture, it provides high power supply rejection and ultralow noise, achieving excellent line and load transient response with only a 10µF ceramic output capacitor.

The ADP7156 regulator typical output noise is 0.9µV RMS from 100Hz to 100kHz and 1.7nV/√Hz for noise spectral density from 10kHz to 1MHz. The ADP7156 is available in a 10-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages, making it not only a very compact solution, but also providing excellent thermal performance for applications requiring up to 1.2A of output current in a small, low-profile footprint.

Table 1-1 Product Description

Part Number	Primary Function	System Function
ADP7156	1.2A, Ultralow Noise, High PSRR, RF Linear Regulator	Provide low-noise, regulated voltage output of 3.3V ± 1.5% within 1.2ms after enable.

Figure 1-1 shows the product specific block diagram of ADP7156.

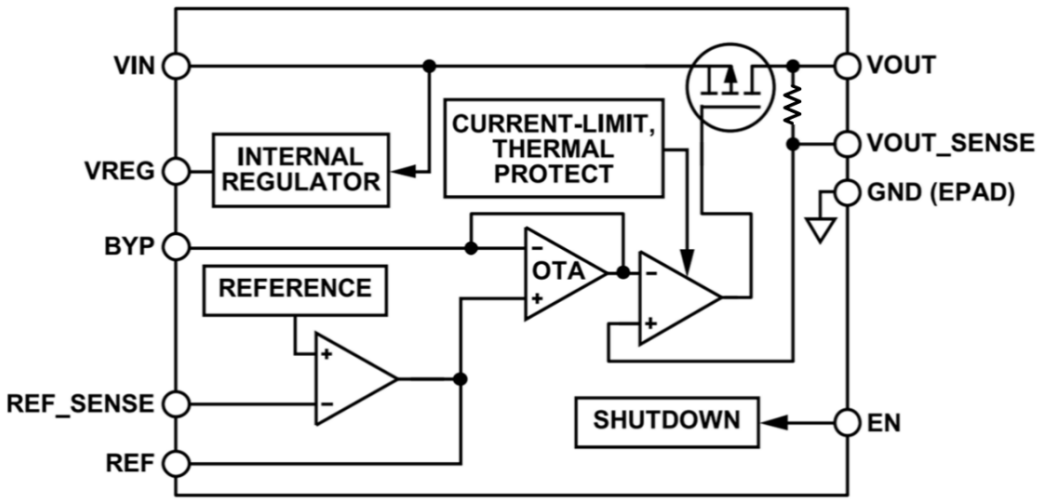

Figure 1-1 ADP7156 Block Diagram

ADP7156 was developed following a quality-managed development process in compliance with the ISO 9001 quality management system standards but was not developed in compliance with the IEC 61508 safety standard. The associated certificates are available on Quality Certificates | Analog Devices.

2 | Functional Safety Failure-In-Time (FIT)

This section offers specific details on the base functional safety failure-in-time (FIT) for the ADP7156, according to SN 29500, IEC 62380 and accelerated testing conditions of high-temperature operating life (HTOL). It also identifies the relevant component category for each standard, allowing customers to compute their own failure rates.

- Table 2-1 provides FIT according to SN 29500
- Table 2-2 provides FIT according to IEC 62380
- Table 2-3 provides FIT according to HTOL

The FIT of ADP7156 based on SN 29500 for a specific industrial mission profile is detailed below:

Table 2-1 Functional Safety Component FIT According to SN 29500

SN 29500 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Predicted Component FIT	99.03

- Mission Profile: 20 years constant operation at 55°C temperature
- Operating Voltage (max): 5.5V
- Power Dissipation: 0.3206W (operating at 0.6A Load)
- Theta-JA: 53.8°C/W

Note 1: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on SN 29500.

- SN 29500 part: Part 2 Table 5 under ASICs
- Sub-category: CMOS, BiCMOS
- Integration Density: 5k-50k
- Part is sensitive to drift

The FIT of ADP7156 based on IEC 62380 for a specific industrial mission profile is detailed below:

Table 2-2 Functional Safety Component FIT According to IEC 62380

IEC 62380 Industrial Mission Profile	FIT (Failures Per 10^9 Hours)
Total Component FIT	7.54
Die FIT	7.15
Package FIT	0.39

Note 2: For applications requiring a different mission profile, the following information can be used to calculate the base FIT based on IEC 62380.

- FIT calculation model: Section 7.3.1, refer to Mathematical Model
- IEC 62380 part and section for die FIT: Table 16, MOS ASIC circuits, Full Custom
- Production year: 2022
- Integration Density: 5k-50k
- Climate type: World-wide (Table 8)
- IEC 62380 part and section for package FIT: Table 17b, Peripheral Connection Packages
- Package type: LFCSP 10 pins, length: 3mm, width: 3mm, pitch: 0.5mm
- Technology Structure: MOS BiCMOS (Low Voltage)
- Substrate Material: Epoxy Glass (FR4, G-10)
- EOS FIT assumed: 0 FIT

The FIT of ADP7156 based on accelerated testing conditions of HTOL is detailed below:

Table 2-3 Functional Safety Component FIT According to HTOL Testing

Confidence Level	FIT (Failures Per 10^9 Hours)
70%	0.12
90%	0.23
95%	0.29
99%	0.45

Note 3: The FIT values for various confidence levels were determined through HTOL reliability studies, utilizing the Arrhenius equation for acceleration assuming a chi-square distribution using the following test parameters:

- Sample size: 57,317
- Number of Failures: 0
- Activation Energy: 0.7eV
- Accelerated Temperature: 55°C
- Equivalent Accelerated Device Hours: 10,155,069,381

3 | Failure Mode Distribution (FMD)

The failure mode distribution includes all relevant failure modes of the product function as defined in the product description.

Table 3-1 shows the failure mode distribution estimation for ADP7156 as derived from the component die area ratio and complexity, and from engineering expertise.

Application Circuit

In this application, power supply connected to the VIN pin operates at 3.8V. The output operates at 3.3V with full load current of 1.2A. VOUT_SENSE pin is connected to VOUT to ensure correct regulation. EN pin is connected to VIN for automatic startup. Other pins such REF, REF_SENSE, BYP, and VREG are configured as shown in Figure 3-1.

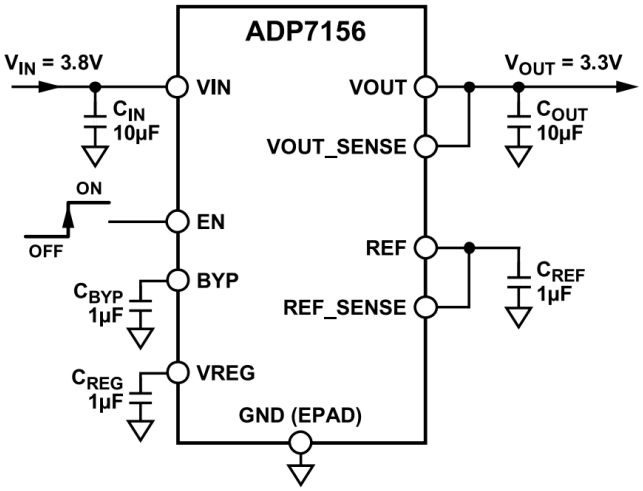

Figure 3-1 ADP7156 Typical Application Circuit

System Function

- Provides low-noise, regulated voltage output of 3.3V ± 1.5% within 1.2ms after enable.

Table 3-1 Failure Mode Distribution

Failure Modes	Failure Mode Distribution
VOUT is off or stuck low close to 0V.[1]	29%
VOUT regulates higher than target.[2]	12%
VOUT regulates lower than target.[3]	9%
VOUT output is oscillating but within regulation.	6%
VOUT is stuck close to VIN.	24%
VOUT settling time > 1.2ms.[4]	3%
VOUT output is oscillating but outside regulation.	1%
No effect on system function.	16%

Note 4:

[1] $0V < VOUT_{actual} < 0.6V$.

[2] $(1.015 \times VOUT_{expected}) < VOUT_{actual} < (VIN - 0.6V)$

[3] $0.6V < VOUT_{actual} < (0.985 \times VOUT_{expected})$.

[4] (VIN - 0.6V) < VOUT < VIN, and tracks VIN. “Tracks VIN” indicates that VOUT changes, either increasing or decreasing, by nearly the same amount as VIN does.

4 | Pin Failure Mode and Effects Analysis (Pin FMEA)

This section presents the Pin Failure Mode and Effects Analysis (Pin FMEA) for ADP7156. The failure modes discussed in this section encompass the common pin-by-pin failure scenarios:

- Pin short-circuited to supply (see Table 4-1)
- Pin short-circuited to GND (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pins (see Table 4-4)

Figure 4-1 illustrates the pin diagram for ADP7156. Refer to the product datasheet for a detailed description of each pin's function.

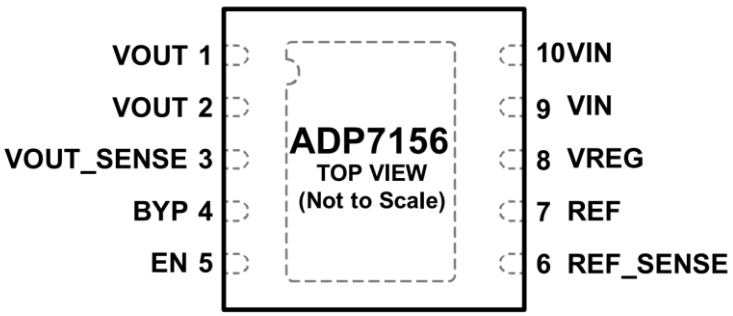

Figure 4-1. ADP7156 Pin Diagram

Below are the usage assumptions and device configuration considered for the Pin FMEA:

- Pin connections were configured as per application circuit. See discussions on section 3.
- The operating voltage range (VIN) is from 2.3V to 5.5V, and the operating temperature range (T_A) is from -40°C to +125°C.

Table 4-1 Pin FMEA for ADP7156 Pins Short-Circuited to Supply

Pin no.	Pin Name	Effect of Failure Mode
1	VOUT1	VOUT is stuck close to VIN.
2	VOUT2	VOUT is stuck close to VIN.
3	VOUT_SENSE	VOUT is stuck close to VIN.
4	BYP	VOUT is stuck close to VIN.
5	EN	Achieves target regulation, but at a higher operating current consumption. No effect.
6	REF_SENSE	VOUT is stuck close to VIN.
7	REF	VOUT is stuck close to VIN.
8	VREG	VOUT regulates higher than target.
9	VIN	This is the typical application circuit. No effect.
10	VIN	This is the typical application circuit. No effect.
11	Exposed Pad	VOUT is off or stuck low close to 0V.

Table 4-2 Pin FMEA for ADP7156 Pins Short-Circuited to GND

Pin no.	Pin Name	Effect of Failure Mode
1	VOUT1	VOUT is off or stuck low close to 0V.
2	VOUT2	VOUT is off or stuck low close to 0V.
3	VOUT_SENSE	VOUT is off or stuck low close to 0V.
4	BYP	VOUT is off or stuck low close to 0V.
5	EN	VOUT is off or stuck low close to 0V.
6	REF_SENSE	VOUT is off or stuck low close to 0V.
7	REF	VOUT is off or stuck low close to 0V.
8	VREG	VOUT is off or stuck low close to 0V.
9	VIN	VOUT is off or stuck low close to 0V.
10	VIN	VOUT is off or stuck low close to 0V.
11	Exposed Pad	This is the typical application circuit. No effect.

Table 4-3 Pin FMEA for ADP7156 Pins Open-Circuited

Pin no.	Pin Name	Effect of Failure Mode
1	VOUT1	Achieves target regulation but expected lifetime is reduced due to over-current stress when output load current is high. No effect on declared system function.
2	VOUT2	Achieves target regulation but expected lifetime is reduced due to over-current stress when output load current is high. No effect on declared system function.
3	VOUT_SENSE	Achieves target regulation but will not compensate IR drop from VOUT pin to load point. No effect.
4	BYP	VOUT output is oscillating but within regulation.
5	EN	VOUT is off or stuck low close to 0V.
6	REF_SENSE	VOUT is stuck close to VIN.
7	REF	VOUT is stuck close to VIN.
8	VREG	VOUT output is oscillating but within regulation.
9	VIN	Achieves target regulation but expected lifetime is reduced due to over-current stress when output load current is high. No effect on declared system function.
10	VIN	Achieves target regulation but expected lifetime is reduced due to over-current stress when output load current is high. No effect on declared system function.
11	Exposed Pad	VOUT is off or stuck low close to 0V.

Table 4-4 Pin FMEA for ADP7156 Pins Short-Circuited to Adjacent Pins

Pin no.	Pin Name	Shorted to	Effect of Failure Mode
1	VOUT1	VOUT2	This is the typical application circuit. No effect.
2	VOUT2	VOUT_SENSE	This is the typical application circuit. No effect.
3	VOUT_SENSE	BYP	VOUT regulates lower than target.
4	BYP	EN	VOUT regulates lower than target.
5	EN	REF_SENSE	VOUT regulates lower than target.
6	REF_SENSE	REF	This is the typical application circuit. No effect.
7	REF	VREG	VOUT regulates higher than target.
8	VREG	VIN	VOUT regulates higher than target.
9	VIN	VIN	This is the typical application circuit. No effect.
10	VIN	VOUT1	VOUT is stuck close to VIN.

5 | Revision History

Revision	Revision Date	Description
A	06Dec25	Initial Release

IMPORTANT NOTES AND DISCLAIMER

PLEASE BE AWARE THAT THE PRODUCT IN QUESTION HAS NOT BEEN DEVELOPED IN ACORDANCE WITH INDUSTRIAL SAFETY STANDARDS AND IS NOT RECOMMENDED FOR SUCH APPLICATIONS AS PER THE SPECIFIC DATA SHEET. THIS REPORT IS INTENDED SOLELY TO PROVIDE THE CUSTOMER WITH DETAILED INFORMATION ON FAILURE MODES AND THEIR DISTRIBUTION ACCORDING TO IEC61508, RELATED TO THE POTENTIAL USE OF QUALITY-MANAGED PARTS FOR SPECIFIC HARDWARE EVALUATION CLASS AS DESCRIBED IN THIS STANDARD.

ANALOG DEVICES AIMS TO ASSIST CUSTOMERS IN DESIGNING AND CREATING THEIR OWN END-PRODUCT SOLUTION THAT COMPLY WITH RELEVANT FUNCTIONAL SAFETY STANDARDS AND REQUIREMENTS. THEREFORE, ANALOG DEVICES DOES NOT GUARANTEE SIL COMPLIANCE AT THE SYSTEM LEVEL. ANALOG DEVICES WILL NOT BE RESPONSIBLE FOR ANY CLAIMS OR DAMAGES ARISING FROM THE CUSTOMER'S USE OF AN ANALOG DEVICES PRODUCT IN LIFE SUPPORT, LIFE-CRITICAL, OR SAFETY-CRITICAL SYSTEMS, EQUIPMENT OR APPLICATIONS. CUSTOMERS WILL INDEMNIFY, DEFEND AND HOLD ANALOG DEVICES HARMLESS FROM ANY CLAIMS, DAMAGES, LOSSES, COSTS, EXPENSES, AND LIABILITIES RESULTING FROM THE USE OF ANY ANALOG DEVICES PRODUCT IN SUCH SYSTEMS, EQUIPMENT, OR APPLICATIONS. ANALOG DEVICES DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THIS DOCUMENTATION AND WILL NOT BE LIABLE FOR ITS CONTENT.

www.analog.com

AHEAD OF WHAT'S POSSIBLE™