

RELIABILITY REPORT
FOR
MXL1543CAI
PLASTIC ENCAPSULATED DEVICES

December 3, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

A handwritten signature in black ink, appearing to read "J Pedicord".

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Quality Assurance
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Reviewed by

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Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MXL1543 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MXL1543 is a three-driver/three-receiver multiprotocol transceiver that operates from a +5V single supply. The MXL1543, along with the MXL1544/MAX3175 and the MXL1344A, form a complete software-selectable data terminal equipment (DTE) or data communication equipment (DCE) interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA-530, EIA-530A, X.21), and V.35 protocols. The MXL1543 transceivers carry the high-speed clock and data signals while the MXL1544/MAX3175 carry the control signals. The MXL1543 can be terminated by the MXL1344A software-selectable resistor termination network or by discrete termination networks.

An internal charge pump and a proprietary low-dropout transmitter output stage allow V.11-, V.28-, and V.35-compliant operation from a +5V single supply. A no-cable mode is entered when all mode pins (M0, M1, and M2) are pulled high or left unconnected. In no-cable mode, supply current decreases to 0.5 μ A and all transmitter and receiver outputs are disabled (high impedance). Short-circuit current limiting and thermal shutdown circuitry protect the drivers against excessive power dissipation.

B. Absolute Maximum Ratings

| <u>Item</u> | <u>Rating</u> |
|--|-----------------------|
| All Voltages Referenced to GND Unless Otherwise Noted. | |
| Supply Voltages | |
| VCC | -0.3V to +6V |
| VDD | -0.3V to +7.3V |
| VEE | +0.3V to -6.5V |
| VDD to VEE (Note 1) | 13V |
| Logic Input Voltages | |
| M0, M1, M2, DCE/DTE, T_IN | -0.3V to +6V |
| Logic Output Voltages | |
| R_OUT | -0.3V to (VCC + 0.3V) |
| Transmitter Outputs | |
| T_OUT_, T3OUT_/R1IN_ | -15V to +15V |
| Short-Circuit Duration | Continuous |
| Receiver Input | |
| R_IN_T3OUT_/R1IN_ | -15V to +15V |
| Operating Temperature Range | |
| MXL1543CAI | 0°C to 70°C |
| Junction Temperature | 150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (T _A = +70°C) | |
| 28-Pin SSOP | 889mW |
| Derates above +70°C | |
| 28-Pin SSOP | 11.1mW/°C |

Note 1: VDD and VEE absolute difference cannot exceed 13V.

II. Manufacturing Information

| | |
|----------------------------------|---|
| A. Description/Function: | +5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers |
| B. Process: | S3 (SG3) Standard 3 micron silicon gate CMOS |
| C. Number of Device Transistors: | 2619 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Philippines or Malaysia |
| F. Date of Initial Production: | January, 2001 |

III. Packaging Information

| | |
|--|---------------------------|
| A. Package Type: | 28-Lead SSOP |
| B. Lead Frame: | Copper |
| C. Lead Finish: | Solder Plate |
| D. Die Attach: | Silver-filled epoxy |
| E. Bondwire: | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | Buildsheet # 05-1901-0241 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 144 x 278 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 3 microns (as drawn) |
| F. Minimum Metal Spacing: | 3 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└─ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 24.13 \times 10^{-9} \quad \lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5669) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS99 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 150\text{mA}$.

Table 1
Reliability Evaluation Test Results

MXL1543CAI

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|-------------|--------------------|
| Static Life Test (Note 1) | | | | |
| | Ta = 135°C Biased Time = 192 hrs. | DC Parameters & functionality | 45 | 0 |
| Moisture Testing (Note 2) | | | | |
| Pressure Pot | Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs. | DC Parameters & functionality | 77 | 0 |
| 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | 77 | 0 |
| Mechanical Stress (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters | 77 | 0 |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic process/package data.

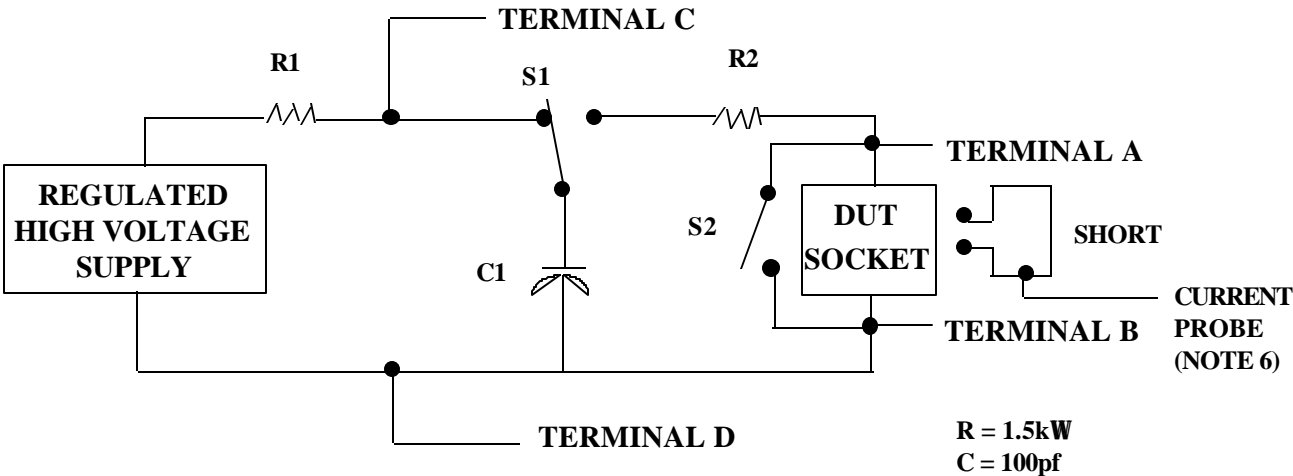
TABLE II. Pin combination to be tested. 1/ 2/

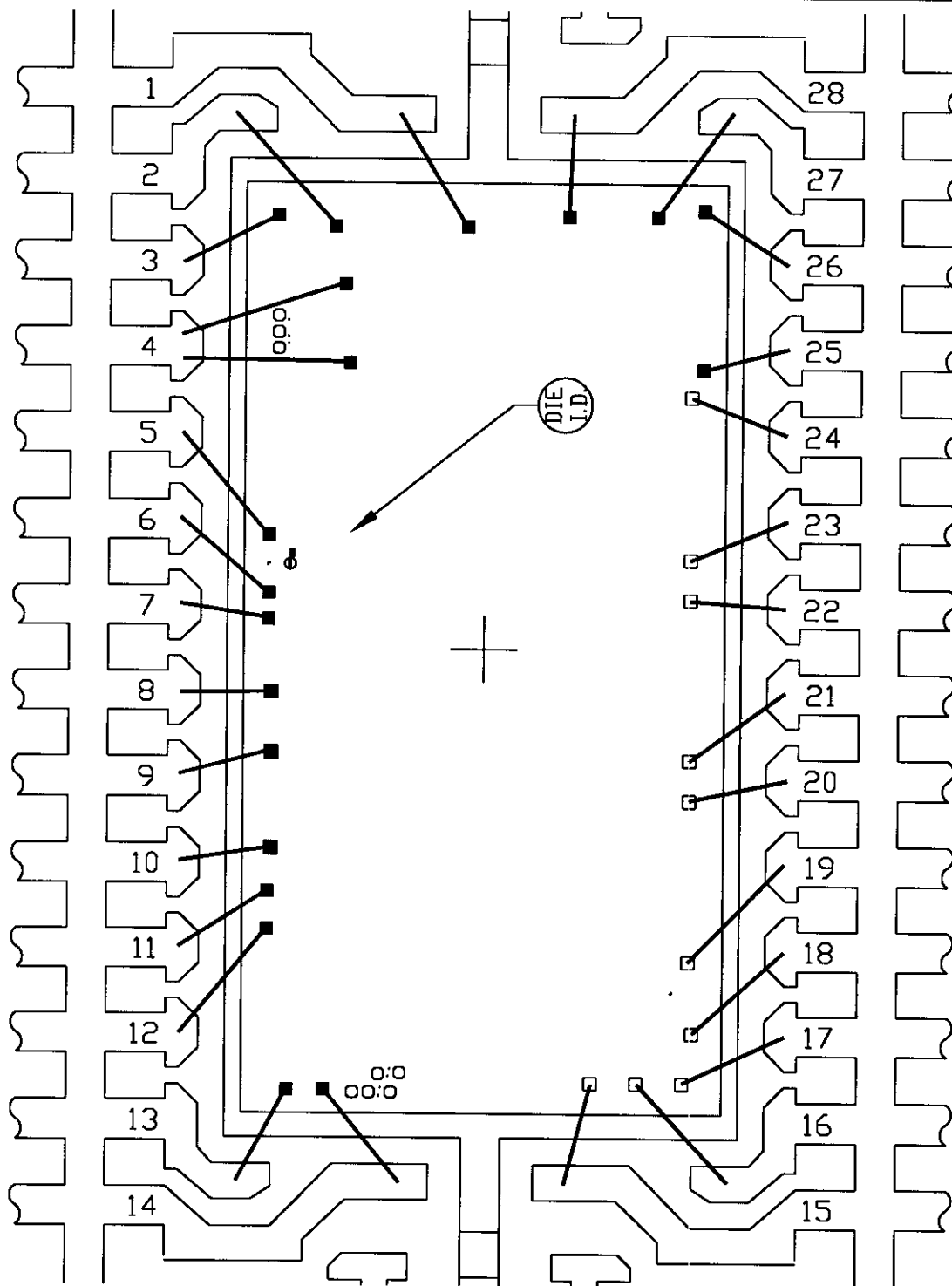
| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except V_{PS1} 3/ | All V_{PS1} pins |
| 2. | All input and output pins | All other input-output pins |

- 1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE:

A28-3

CAV./PAD SIZE:

154X291

PKG.

DESIGN

SIGNATURES

DATE

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BOND DIAGRAM #:

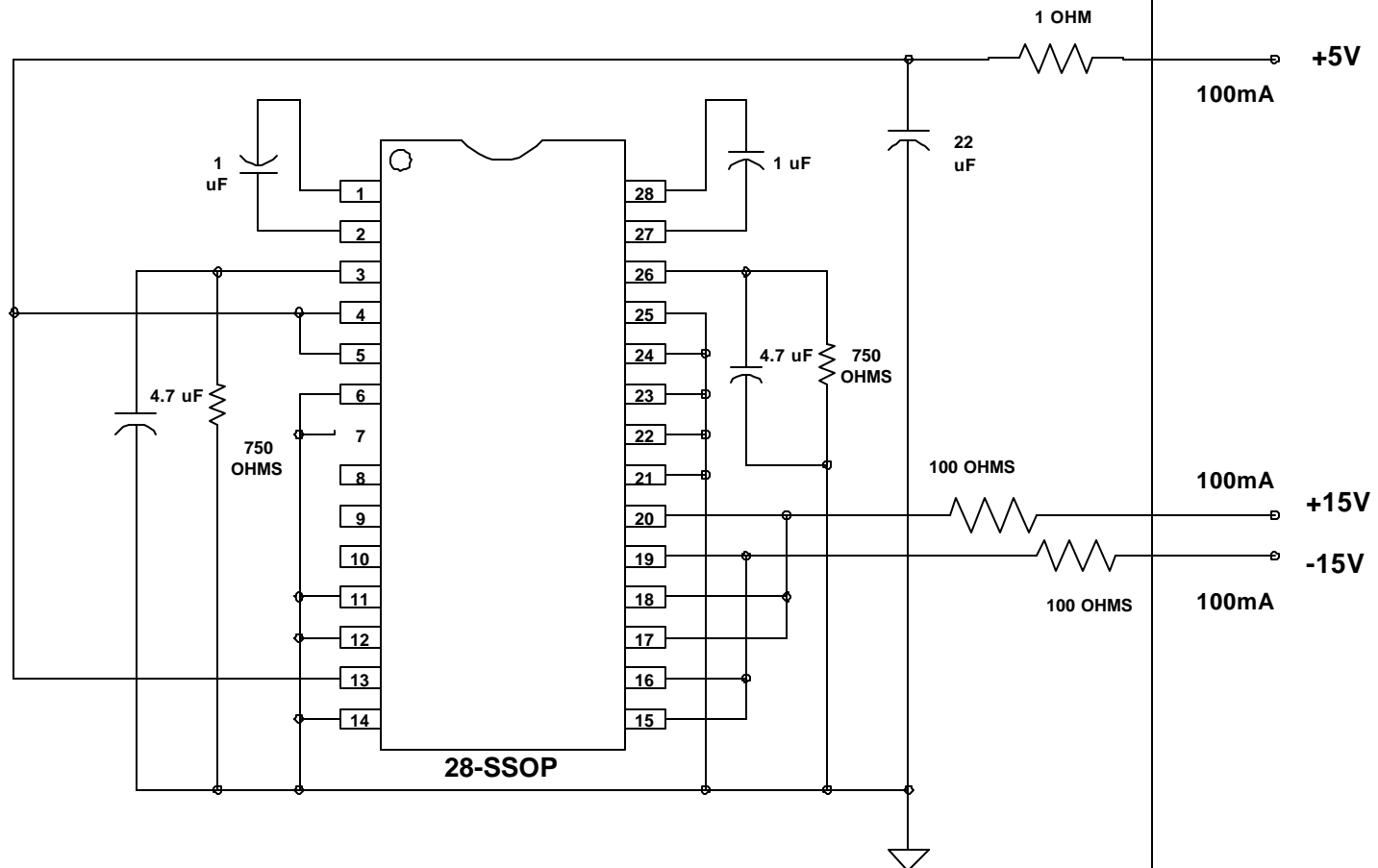
05-1901-0241

REV:

A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MXL 1543

MAX. EXPECTED CURRENT = 100mA

DRAWN BY: HAK TAN

NOTES: