RELIABILITY REPORT

FOR

MXD1815xRxx

PLASTIC ENCAPSULATED DEVICES

February 22, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by	Reviewed by
Jim Pedicord Quality Assurance Reliability Lab Manager	Bryan J. Preeshl Quality Assurance Executive Director

Conclusion

The MXD1815 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MXD1815 microprocessor (µP) reset circuit monitors power supplies in µP and digital systems. This device provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +2.5V/+3.0V/+3 systems.

This circuit asserts a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping reset asserted for at least 100ms after V_{CC} rises above the reset threshold.

The MXD1815 (push-pull) has an active-low RESET-bar output.

The MXD1815 is guaranteed to output the correct logic state for V_{CC} down to +1V. This IC provide a reset comparator designed to ignore fast transients on V_{CC}. Reset thresholds are available between +2.18V and +4.62V. This small, low-power (4µA) device is ideal for use in portable equipment. This device is available in space-saving 3-pin SC70 and SOT23 packages, and is specified from -40°C to +105°C.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6V
Push-Pull /RESET to GND	-0.3V to (VCC + 0.3V)
Input Current (VCC, /RESET)	20mA
Output Current (/RESET)	20mA
Operating Temperature Range	-40°C to +105°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Power Dissipation	
3-Pin SC70	174mW
3-Pin SOT	320mW
Derates above +70°C	
3-Pin SC70	2.17mW/°C
3-Pin SOT	4.00mW/°C

II. Manufacturing Information

A. Description/Function: Low-Power uP Reset Circuit

B. Process: S8 - Standard 8 micron silicon gate CMOS

C. Number of Device Transistors: 709

D. Fabrication Location: California, USA

E. Assembly Location: Philippines

F. Date of Initial Production: October, 2001

III. Packaging Information

A. Package Type:	**3-Lead SC70**	**3-Lead SOT23**
B. Lead Frame:	Alloy 42	Copper or Alloy 42
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0145	Buildsheet # 05-1601-0144
H. Flammability Rating:	Class UL94-V0	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 31 X 30 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: TiW/ AlCu/ TiWN

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times \underset{\uparrow}{4389} \times 80 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-5804) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS52-4 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MXD1815xRxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SC70 SOT23	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data

Attachment #3

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

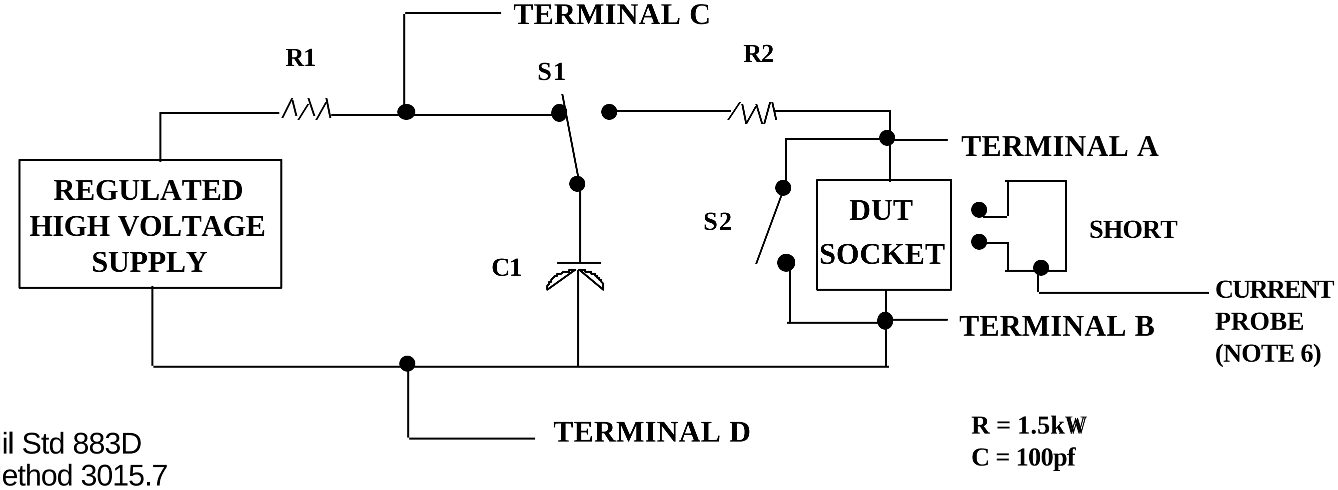
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_S$, V_{REF}, etc).

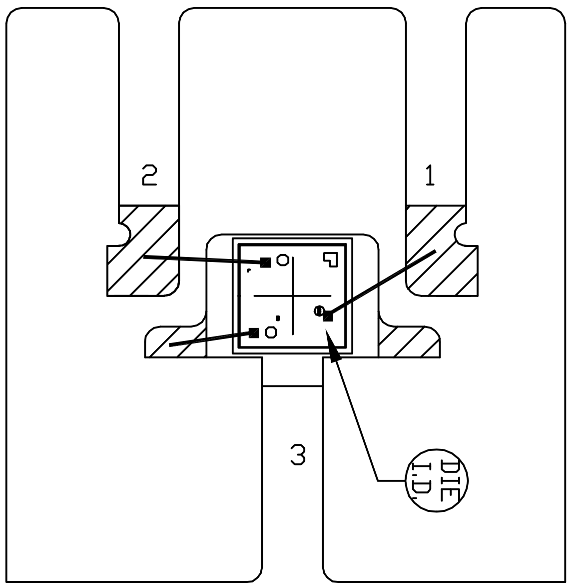
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

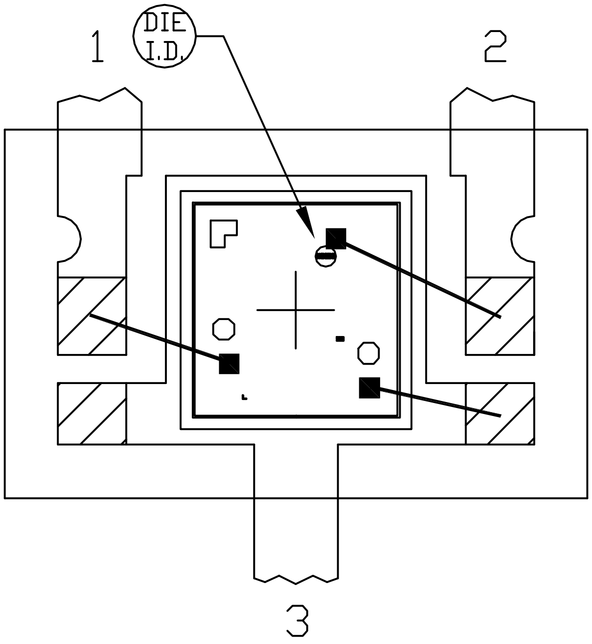
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





▨ BONDING AREA

PKG. CODE: U3-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 45x32	PKG.		3/5/01	BOND DIAGRAM #: 05-1601-0144	REV: A
	DESIGN		3/6/01		



SCALE: 40x

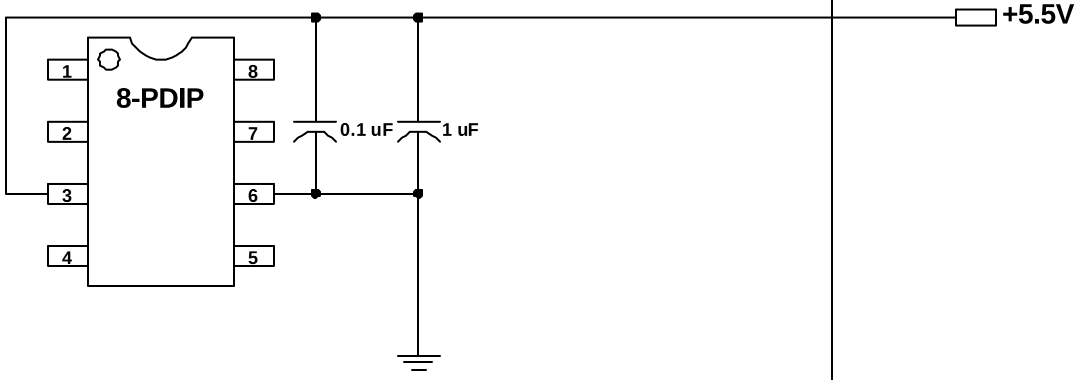
CAVITY DOWN

▨ BONDABLE AREA

PKG. CODE: X3-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 34x35	PKG.		3/5/01	BOND DIAGRAM #: 05-1601-0145	REV: A
	DESIGN		3/6/01		

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MXD 1810/1811/1812/1813/1815/1816/ 1817/1818

MAX. EXPECTED CURRENT = 10mA

DRAWN BY: HAK TAN

NOTES: