

RELIABILITY REPORT
FOR
MAX9979Xxxx+
PLASTIC ENCAPSULATED DEVICES

August 10, 2009

MAXIM INTEGRATED PRODUCTS

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Approved by
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Conclusion

The MAX9979Xxxx+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	IV.Die Information
.....Attachments	

I. Device Description

A. General

The MAX9979 fully integrated, high performance, dual-channel pin electronics integrate multiple Automatic Test Equipment (ATE) functions into a single IC including Driver, Comparator, Load (DCL), Parametric Measurement Unit (PMU), and built-in (16-bit) level setting Digital-to-Analog Converters (DACs). The device is ideal for memory and SOC tester applications. Each channel includes a three-level pin driver, a window comparator, a differential comparator, dynamic clamps, a versatile PMU, an active load, a high voltage (VHH) programmable level and fourteen independent level setting DACs. The MAX9979 features programmable cable droop compensation for the driver output and for the comparator input, adjustable driver output resistance that allows optimal performance over typical data path transmission line variations, slew-rate adjustment, and a programmable high voltage driver output. The MAX9979 Driver features a wide 8V (-1.5V to +6.5V) high speed operating voltage range and a VHH programmable range of up to +13V. Operation modes include High-Impedance (High-Z), Active Termination (3rd Level Drive) and VHH (4TH Level Drive) modes. The device is highly linear even at low voltage swings. The driver provides high-speed differential control inputs compatible with most high-speed logic families. The window comparators provide open-collector outputs and extremely low timing variation over changes in slew rate, pulse width and overdrive voltage. In High-Z mode, the MAX9979 features dynamic clamps that dampen high-speed Device Under Test (DUT) waveforms. The 20mA Active Load facilitates fast contact testing when used in conjunction with the comparators, and functions as a pull-up/pull-down for open-drain/collector DUT outputs. The PMU offers five current ranges from $\pm 2.0\mu\text{A}$ to $\pm 50\text{mA}$ and can force and measure current or voltage. An SPI compatible serial interface configures the MAX9979. The MAX9979 is available in the small footprint 68-pin 10x10x1.00mm TQFN-EP-IDP package with exposed pad on the top for easy heat removal. Power dissipation is typically 1.2W per channel over the full operating voltage range with the active load disabled. The MAX9979 operates over an internal die temperature range of +40°C to +100°C and provides a temperature monitor output.

II. Manufacturing Information

A. Description/Function:	Dual Driver/Comparator/Load/PMU with Integrated Level Setting DACs with Calibration for Gain and Offset (CALDACs), VHH Programming, Programmable Output Impedance, Cable Droop Compensation, and Slew Rate Adjustment
B. Process:	CB4
C. Number of Device Transistors:	72683
D. Fabrication Location:	Oregon
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	4/25/2008

III. Packaging Information

A. Package Type:	68 Pin TQFN 10x10x0.8mm Pb-Free
B. Lead Frame:	Cu Alloy
C. Lead Finish:	Matte Sn Plate
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3

IV. Die Information

A. Dimensions:	270 X 270 mils
B. Passivation:	Si ₃ N ₄ (Silicon nitride)
C. Interconnect:	Gold
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

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|-----------------------------------|---|
| A. Quality Assurance Contacts: | Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 10.6 \times 10^{-9}$$

$$\lambda = 10.6 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the CB4 Process results in a FIT Rate of 0.14 @ 25C and 2.42 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AT23-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX9979Xxxx+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Tj = 150°C Biased Time = 1000 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data