

RELIABILITY REPORT  
FOR  
**MAX988EUK**  
PLASTIC ENCAPSULATED DEVICES

June15, 2006

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

Written by

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## Conclusion

The MAX988 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX988 single/dual/quad micropower comparator features low-voltage operation and Rail-to-Rail inputs and outputs. It's operating voltage ranges from +2.5V to +5.5V, making them ideal for both 3V and 5V systems. This comparator also operates with  $\pm 1.25V$  to  $\pm 2.75V$  dual supplies. It consumes only 48 $\mu A$  per comparator while achieving a 120ns propagation delay.

The common-mode input voltage range extends 250mV beyond the supply rails. Input bias current is typically 1.0pA, and input offset voltage is typically 0.5mV. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The output stage's unique design limits supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The MAX988/MAX992/MAX996 have an open-drain output stage that can be pulled beyond  $V_{CC}$  to 6V (max) above  $V_{EE}$ . These open-drain versions are ideal for level translators and bipolar to single-ended converters.

The single MAX988 is available in tiny 5-pin SOT23 package.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage (VCC to VEE)	6V
IN <sub>-</sub> , IN <sub>+</sub> to VEE	-0.3V to (VCC + 0.3V)
OUT <sub>-</sub> to VEE	
MAX987/MAX991/MAX995	-0.3V to (VCC + 0.3V)
MAX988/MAX992/MAX996	-0.3V to 6V
OUT <sub>-</sub> Short-Circuit Duration to VEE or VCC	10s
Continuous Power Dissipation (TA = +70°C)	
5-Pin SC70 (derate 3.1mW/°C above +70°C)	247mW
5-Pin SOT23 (derate 7.10mW/°C above +70°C)	571mW
8-Pin SOT23 (derate 9.1mW/°C above +70°C)	727mW
8-Pin SO (derate 5.88mW/°C above +70°C)	471mW
8-Pin $\mu$ MAX (derate 4.5mW/°C above +70°C)	362mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C)	727mW
14-Pin SO (derate 8.33mW/°C above +70°C)	667mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

## II. Manufacturing Information

- A. Description/Function: High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators
- B. Process: B12 (Standard 1.2 micron silicon gate CMOS)
- C. Number of Device Transistors:
- D. Fabrication Location: California or Oregon, USA
- E. Assembly Location: Malaysia, Philippines or Thailand
- F. Date of Initial Production: July, 1997

## III. Packaging Information

- A. Package Type: **5-Pin SOT23**
- B. Lead Frame: Copper or Alloy 42
- C. Lead Finish: 100% Matte Tin
- D. Die Attach: Non Conductive
- E. Bondwire: Gold (1 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-1501-0201
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

## IV. Die Information

- A. Dimensions: 56 x 38 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 1.2 microns (as drawn)
- F. Minimum Metal Spacing: 1.2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{SiO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.73 \times 10^{-9}$$

$$\lambda = 13.73 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5255) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B12/S12 Process results in a FIT rate of 0.10 @ 25°C and 1.78 @ 55°C (eV = 0.8, UCL = 60%).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The CM61-3 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX988EUK**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test (Note 1)</b>					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
<b>Moisture Testing (Note 2)</b>					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress (Note 2)</b>					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

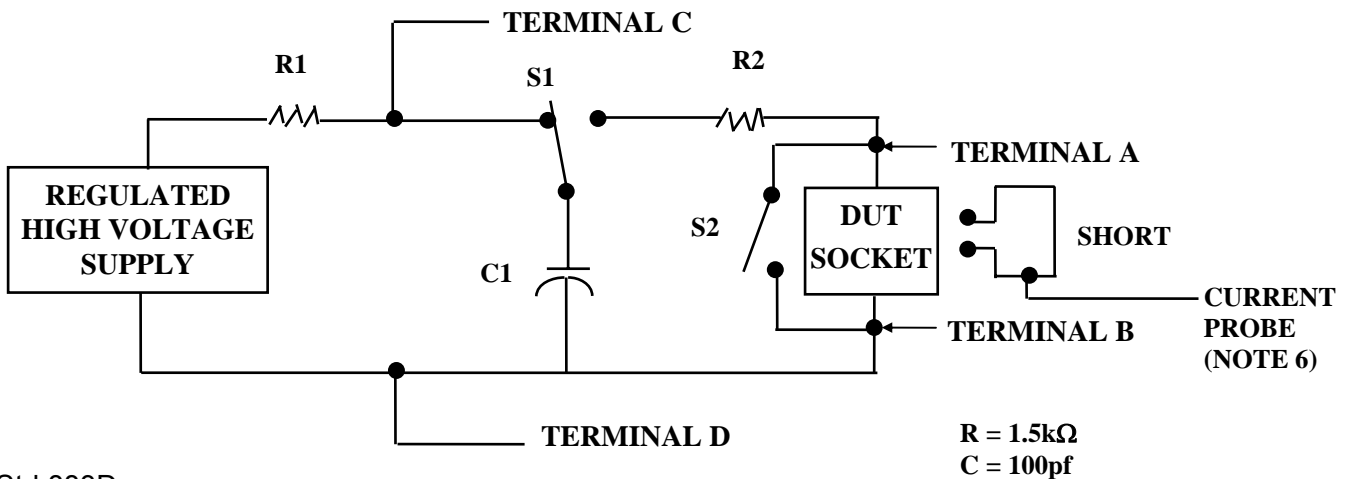
2/ No connects are not to be tested.

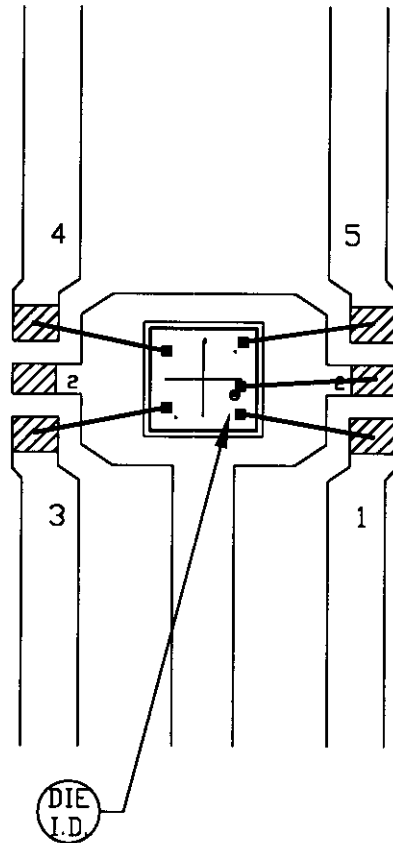
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





USE NON-CONDUCTIVE EPOXY  
 ▨ - BONDING AREA

NOTE: CAVITY DOWN

PKG. CODE: U5-1	
CAV./PAD SIZE: 64X45	PKG. DESIGN

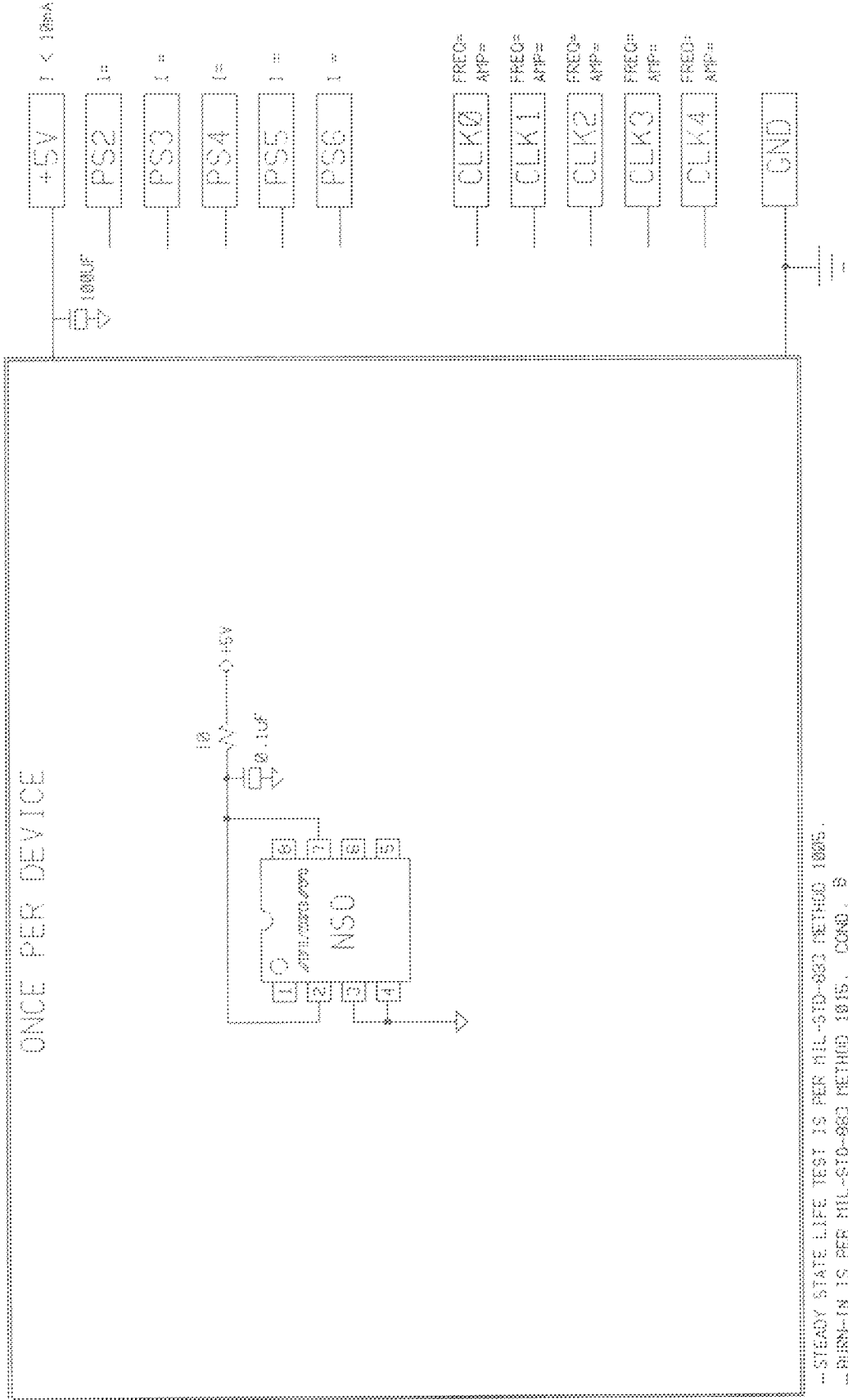
SIGNATURES

DATE

<b>MAXIM</b> CONFIDENTIAL & PROPRIETARY	
BOND DIAGRAM #: 05-1501-0201	REV: B

ONCE PER BOARD

ONCE PER DEVICE



--STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.  
 --BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. 9

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR CXJ COMMERCIAL [X] HR/983

SPEC. NO. 06-5255 REV: A

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

DATE: 12/18/96

MAX985/6/7/8