

FOR
MAX98303EWE+

July 26, 2013

WAFER LEVEL PRODUCTS

MAXIM INTEGRATED

160 RIO ROBLES SAN JOSE, CA 95134

Approved by				
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Quality Assurance				
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Conclusion

The MAX98303EWE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX98303 stereo 3.1W Class D amplifier provides Class AB audio performance with Class D efficiency. This device offers five selectable gain settings (6dB, 9dB, 12dB, 15dB, and 18dB) set by a single gain-select input (GAIN). Active emissions limiting, edge-rate, and overshoot control circuitry greatly reduces EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices. These features reduce application component count. The IC's 2.0mA at 3.7V, 2.7mA at 5V, quiescent current extends battery life in portable applications. The IC is available in a 16-bump WLP (1.68mm x 1.68mm x 0.64mm) package specified over the extended -40°C to +85°C temperature range.



II. Manufacturing Information

A. Description/Function: Stereo 3.1W Class D Amplifier

B. Process: \$18
C. Number of Device Transistors: 6607
D. Fabrication Location: California
E. Assembly Location: Texas

F. Date of Initial Production: September 24, 2010

III. Packaging Information

A. Package Type: 16 bmp WLP

B. Lead Frame: N/A
C. Lead Finish: N/A
D. Die Attach: N/A
E. Bondwire: N/A
F. Mold Material: N/A

G. Assembly Diagram: #05-9000-4202H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: N/A
K. Single Layer Theta Jc: N/A
L. Multi Layer Theta Ja: 58°C/W
M. Multi Layer Theta Jc: N/A

IV. Die Information

A. Dimensions: 66.14 X 66.14 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

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C. Interconnect: Al with Ti/TiN Barrier

D. Backside Metallization: NoneE. Minimum Metal Width: 0.18umF. Minimum Metal Spacing: 0.18um

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO₂I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)

Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm
D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (3) is calculated as follows:

$$x = 22.9 \times 10^{-9}$$

% = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SQ1ZBQ001B, DC 1027)

The AX47 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.



Table 1Reliability Evaluation Test Results

MAX98303EWE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (No	ote 1) Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SQ1ZBQ001B, D/C 1027

Note 1: Life Test Data may represent plastic DIP qualification lots.