

RELIABILITY REPORT  
FOR  
MAX9820ETB+  
PLASTIC ENCAPSULATED DEVICES

July 8, 2011

**MAXIM INTEGRATED PRODUCTS**

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<b>Approved by</b>
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Quality Assurance
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## Conclusion

The MAX9820ETB+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX9820 Windows Vista®-compliant stereo headphone amplifier is designed for portable equipment where board space is at a premium. It features Maxim's DirectDrive® architecture to produce a ground-referenced output from a single supply, eliminating the large output-coupling capacitors required by conventional single-supply headphone amplifiers. The MAX9820 features an undervoltage lockout that prevents over discharging of the battery during brownout conditions, click-and-pop suppression that eliminates audible transients on startup, a low-power shutdown mode, and thermal-overload and short-circuit protection. Additionally, the MAX9820 suppresses RF radiation received by input and supply traces acting as antennas and prevents the amplifier from demodulating the coupled noise. The MAX9820 is available in a 10-pin TDFN package (3mm x 3mm x 0.8mm) and specified over the -40°C to +85°C extended temperature range.

## II. Manufacturing Information

A. Description/Function:	DirectDrive Headphone Amplifier with External Gain
B. Process:	S45
C. Number of Device Transistors:	2200
D. Fabrication Location:	Texas
E. Assembly Location:	China
F. Date of Initial Production:	July 9, 2009

## III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3289
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	9°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	9°C/W

## IV. Die Information

A. Dimensions:	41 X 58 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot TOWZCQ001C D/C 0918)

The AU96 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX9820ETB+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TOWZCQ001C, D/C 0918

Note 1: Life Test Data may represent plastic DIP qualification lots.