

RELIABILITY REPORT
FOR
MAX97003EWP+T
WAFER LEVEL PRODUCTS

September 30, 2015

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX97003EWP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX97003 audio subsystem combines a mono speaker amplifier with a stereo headphone amplifier. The headphone and speaker amplifiers have independent volume and on/off controls. The four inputs are configurable as two differential or four single-ended inputs. To minimize output noise, both the headphone and speaker outputs utilize a downward expander/noise gate to attenuate noise when no desired input signal is present. The speaker output incorporates an adjustable dynamic range compressor (DRC) and distortion limiter to protect the speaker and maximize loudness. This allows high gain for low-level signals without compromising the quality of large signals. All controls are performed using the two-wire I²C interface. The IC operates in the extended -40°C to +85°C temperature range, and is available in the 2.0mm x 2.4mm, 20-bump WLP package (0.4mm pitch).

II. Manufacturing Information

A. Description/Function:	High-Efficiency, Low-Noise Audio Subsystem
B. Process:	S18
C. Number of Device Transistors:	137065
D. Fabrication Location:	California
E. Assembly Location:	Texas
F. Date of Initial Production:	September 23, 2011

III. Packaging Information

A. Package Type:	20 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A
F. Mold Material:	
G. Assembly Diagram:	#05-9000-4422
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	46°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	93.70X77.56 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SOKZDQ002B, D/C 1132)

The AX57 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX97003EWP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SOKZDQ002C, D/C 1132

Note 1: Life Test Data may represent plastic DIP qualification lots.