RELIABILITY REPORT

FOR

MAX9650

PLASTIC ENCAPSULATED DEVICES

March 8, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX9650ATA+/MAX9650AZK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9650/MAX9651 are single- and dual-channel VCOM amplifiers with rail-to-rail inputs and outputs. The MAX9650/MAX9651 can drive up to 1300mA of peak current per channel and operate up to 20V. The MAX9650/MAX9651 are designed to source and sink a high current quickly to hold the VCOM voltage stable in large TFT-LCD panels. The MAX9650/MAX9651 feature 40V/µs slew rate and 35MHz bandwidth to quickly settle outputs for 120Hz frame rate and full HD television. The MAX9650/MAX9651 feature output short-circuit protection and thermal shutdown. These devices are available in exposed pad packages for excellent heat dissipation

II. Manufacturing Information

A. Description/Function:	High Current and Fast Settling Time to Quickly Restore VCOM Voltage for TFT LCDs	
B. Process:	S4	
C. Number of Device Transistors:	147	
D. Fabrication Location:	Texas or Japan	
E. Assembly Location:	Thailand, Malaysia or China	Malaysia
F. Date of Initial Production:	July 25, 2008	

III. Packaging Information

A. Package Type:	8-pin TDFN 3x3	5-pin TSOT
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive Epoxy	Conductive Epoxy
E. Bondwire:	Au (1.3 mil dia.)	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3406	#05-9000-3267
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	54°C/W	
K. Single Layer Theta Jc:	8.3°C/W	
L. Multi Layer Theta Ja:	41°C/W	
M. Multi Layer Theta Jc:	8.3°C/W	

IV. Die Information

A. Dimensions:	38 X 40 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/Cu (Cu = 0.5%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4 Process results in a FIT Rate of 0.28 @ 25C and 4.85 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The DV15 die type has been found to have all pins able to withstand an ESD transient pulse of

HBM: +/- 2500V per JEDEC JESD22-A114
CDM: +/- 750V per JEDEC JESD22-C101
MM: +/- 250V per JEDEC JESD22-A115

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX9650ATA+/MAX9650AZK+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data