RELIABILITY REPORT

FOR

MAX9390EHJ+T

PLASTIC ENCAPSULATED DEVICES

April 18, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineer

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Conclusion

The MAX9390EHJ+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9390/MAX9391 dual 2 x 2 crosspoint switches perform high-speed, low-power, and low-noise signal distribution. The MAX9390/MAX9391 multiplex one of two differential input pairs to either or both low-voltage differential signaling (LVDS) outputs for each channel. Independent enable inputs turn on or turn off each differential output pair. Four LVCMOS/LVTTL logic inputs (two per channel) control the internal connections between inputs and outputs. This flexibility allows for the following configurations: 2 x 2 crosspoint switch, 2:1 mux, 1:2 splitter, or dual repeater. This makes the MAX9390/MAX9391 ideal for protection switching in fault-tolerant systems, loopback switching for diagnostics, fanout buffering for clock/data distribution, and signal regeneration. Fail-safe circuitry forces the outputs to a differential low condition for undriven inputs or when the common-mode voltage exceeds the specified range. The MAX9390 provides high-level input fail-safe detection for LVDS, HSTL, and other GND-referenced differential inputs. The MAX9391 provides low-level input fail-safe detection for LVPECL, CML, and other VCC-referenced differential inputs. Ultra-low 82ps(P-P) (max) pseudorandom bit sequence (PRBS) jitter ensures reliable communications in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery, or serializers and deserializers. The high-speed switching performance guarantees 1.5GHz operation and less than 65ps (max) skew between channels. LVDS inputs and outputs are compatible with the TIA/EIA-644 LVDS standard. The LVDS outputs drive 100 loads. The MAX9390/MAX9391 are offered in a 32-pin TQFP package and operate over the extended temperature range (-40°C to +85°C). Also refer to the MAX9392/MAX9393 with flow-through pinout.

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II. Manufacturing Information

A. Description/Function:	Anything-to-LVDS Dual 2 x 2 Crosspoint Switches
B. Process:	GST2
C. Fabrication Location:	USA
D. Assembly Location:	Philippines
E. Date of Initial Production:	April 26, 2003

III. Packaging Information

A. Package Type:	32-pin TQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0478
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	76.4°C/W
M. Multi Layer Theta Jc:	18.9°C/W

IV. Die Information

A. Dimensions:	98X73 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 21.99 \times 10^{-9}$

λ = 21.99 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the GST2 Process results in a FIT Rate of 0.06 @ 25°C and 1.10 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The EC35 die type has been found to have all pins able to withstand an HBM transient pulse of 2500 per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX9390EHJ+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	50	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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