RELIABILITY REPORT

FOR

MAX9370EUA+

PLASTIC ENCAPSULATED DEVICES

August 22, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX9370EUA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9370/MAX9371/MAX9372 LVTTL/TTL-to-differential LVPECL/PECL translators are designed for high-speed communication signal and clock driver applications. The MAX9370/MAX9372 are dual LVTTL/TTL-to-LVPECL/PECL translators that operate in excess of 1GHz. The MAX9371 is a single translator. The MAX9370/MAX9371 operate over a wide 3.0V to 5.25V supply range, allowing high-performance clock or data distribution in systems with a nominal 3.3V or 5.0V supply. The MAX9372 is designed to operate from 3.0V to 3.6V. The devices default to output high if the input is disconnected. They feature low 270ps propagation delay. The MAX9370/MAX9371/MAX9372 employ industry-standard flow-through pinouts. These devices are specified for operation from -40°C to +85°C, and are offered in space-saving, 8-pin SOT23, µMAX, and SO packages.

II. Manufacturing Information

A. Description/Function:	LVTTL/TTL-to-Differential LVPECL/PECL Translators
B. Process:	GST2
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines, Thailand, or Malaysia
F. Date of Initial Production:	April 27, 2002

III. Packaging Information

A. Package Type:	8-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-3601-0032
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	221°C/W K.
Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	206.3°C/W
M. Multi Layer Theta Jc:	41.9°C/W

IV. Die Information

A. Dimensions:	46 X 30 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9706 \times 90 \times 2}$$ (Chi square value for MTTF upper limit)

(where 9706 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 5.5 \times 10^{-9}$

$\lambda = 5.5$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the GST2 Process results in a FIT Rate of 0.03 @ 25C and 0.48 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot N7L0BQ002B, D/C 0225)

The EC19 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX9370EUA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 150°C	DC Parameters	45	0	N7L0BQ002B, D/C 0225
	Biased	& functionality	45	0	N7L0AQ001B, D/C 0206
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.