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RELIABILITY REPORT

FOR

MAX9360EKA+

PLASTIC ENCAPSULATED DEVICES

July 27, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

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Conclusion

The MAX9360EKA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX9360/MAX9361 are low-skew, single LVTTL/TTL/CMOS-to-differential LVECL/ECL translators designed for high-speed signal and clock driver applications. For interfacing to LVTTL/TTL/CMOS input signals, these devices operate over a 3.0V to 5.5V supply range, allowing high-performance clock or data distribution. For interfacing to differential LVECL/ECL output signals, these devices operate from a -2.375V to -5.5V supply. The MAX9360 is a 3.3V LVTTL/CMOS-to-LVECL/ECL translator that operates at a typical speed of 3GHz. The MAX9361 is a 5V TTL/CMOS-to-LVECL/ECL translator that operates at a typical speed of 1.3GHz. Both devices can be used to drive either LVECL devices or standard ECL devices with a negative supply range of -2.375V to -5.5V. The devices default to high if the input is disconnected, and feature ultra-low propagation delay: 440ps for the MAX9360, 810ps for the MAX9361.

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II. Manufacturing Information

A. Description/Function:	LVTTL/TTL/CMOS-to-Differential LVECL/ECL Translators
B. Process:	GST2
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Thailand
F. Date of Initial Production:	January 26, 2002

III. Packaging Information

A. Package Type:	8-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-3601-0015
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Jb:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	195.8°C/W
M. Multi Layer Theta Jc:	70°C/W

IV. Die Information

A. Dimensions:	43X30 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9706 \times 90 \times 2}$$ (Chi square value for MTTF upper limit)

(where 9706 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 5.46 \times 10^{-9}$

λ = 5.46 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the GST2 Process results in a FIT Rate of 0.06 @ 25C and 1.08 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot N5Y0CQ002A, D/C 0220)

The EC10 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-50mA.

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Table 1

Reliability Evaluation Test Results

MAX9360EKA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45 45	0 0	N5Y0CQ002A, D/C 0220 N5Y0BQ001B, D/C 0149

Note 1: Life Test Data may represent plastic DIP qualification lots.

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