RELIABILITY REPORT

FOR

MAX9323ExP

PLASTIC ENCAPSULATED DEVICES

April 2, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX9323 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9323 low-skew, low-jitter, clock and data driver distributes one of two single-ended LVCMOS inputs to four differential LVPECL outputs. A single logic control signal (CLK_SEL) selects the input signal to distribute to all outputs. The device operates from 3.0V to 3.6V, making the device ideal for 3.3V systems, and consumes only 25mA (max) of supply current.

The MAX9323 features low 150ps part-to-part skew, low 11ps output-to-output skew, and low 1.7ps RMS jitter, making the device ideal for clock and data distribution across a backplane or board. All outputs are enabled and disabled synchronously with the clock input to prevent partial output clock pulses.

The MAX9323 is available in space-saving 20-pin TSSOP and ultra-small 20-pin 4mm x 4mm thin QFN packages and operates over the extended (-40°C to +85°C) temperature range. The MAX9323 is pin compatible with Integrated Circuit Systems' ICS8535-01

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +4.0V
Q_, Q_, CLK_, CLK_SEL, CLK_EN to GND	-0.3V to (VCC + 0.3V)
Continuous Output Current	50mA
Surge Output Current	100mA
Junction-to-Ambient Thermal Resistance in Still Air	
20-Pin TSSOP	+91°C/W
20-Pin 4mm . 4mm Thin QFN	+59.3°C/W
Junction-to-Case Thermal Resistance	
20-Pin TSSOP	+20°C/W
20-Pin 4mm . 4mm Thin QFN	+2°C/W
Operating Temperature Range	-40°C to +85°C
Junction Temperature.	+150°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
20-Pin TSSOP	879mW
20-Pin 4mm . 4mm Thin QFN	1349mW
Derates above +70°C	
20-Pin TSSOP	11mW/°C
20-Pin 4mm . 4mm Thin QFN	16.9mW/°C

II. Manufacturing Information

A. Description/Function:	One-to-Four LVCMOS-to-LVPECL Output Clock and Data Driver
B. Process:	MB20 Bi-CMOS Process
C. Number of Device Transistors:	4430
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea, Malaysia, Philippines or Thailand
F. Date of Initial Production:	August, 2002

III. Packaging Information

	20-Pin TSSOP	**20-Pin QFN**
A. Package Type:		
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0067	# 05-9000-0070
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	52 x 65 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5.0 mil.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.78 \times 10^{-9}$ $\lambda = 10.78$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-6046 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The EC27 die type has been found to have all pins able to withstand a transient pulse of <200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

. Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX9323ExP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification packages.
Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

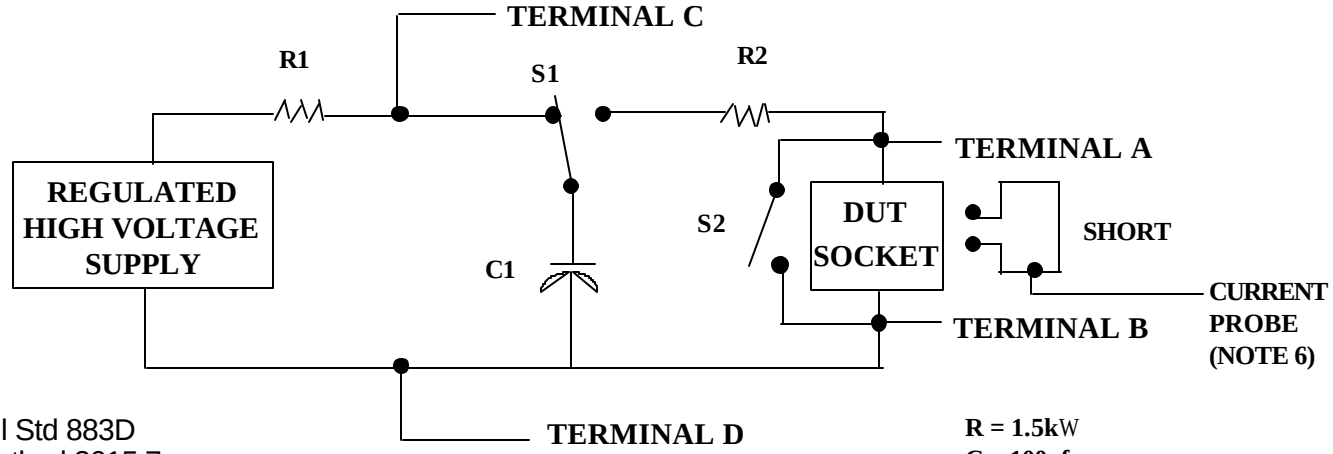
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8