



RELIABILITY REPORT
FOR
MAX9266GCM/V+T
PLASTIC ENCAPSULATED DEVICES

November 29, 2011

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX9266GCM/V+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9266 gigabit multimedia serial link (GMSL) deserializer features an LVDS system interface and high-bandwidth digital content protection (HDCP) decryption for content protection of DVD and Blu-ray(tm) video and audio data. The deserializer pairs with any HDCP-GMSL serializer to form a digital serial link for the transmission of control data and HDCP-encrypted video and audio data. GMSL is an interface approved by Digital Content Protection, LLC (DCP). The deserializer features 3-channel and 4-channel modes. The 3-channel mode outputs three lanes of LVDS data (21 bits), UART control signals, and three audio outputs. The 4-channel mode outputs four lanes of LVDS data (28 bits), UART control signals, three audio outputs, and auxiliary control signals. The three audio outputs are for I²S audio, supporting an 8kHz to 192kHz sampling frequency and a sample depth of 4 to 32 bits. The embedded control channel forms a full-duplex differential 9.6kbps to 1Mbps UART link between the serializer and the deserializer. An electronic control unit (ECU) or microcontroller (μ C) can be located on the serializer side of the link (typical for video display), on the deserializer side of the link (typical for image sensing), or on both sides. The control channel enables ECU/ μ C control of peripherals on the remote side, providing such functions as backlight control, touch-screen input, and HDCP-related operations. The serial link signaling is AC-coupled current-mode logic (CML) with scrambled 8b/10b coding. For driving longer cables, GMSL serializers have programmable pre/deemphasis, and the deserializer has a programmable channel equalizer. For reduced EMI, the deserializer has programmable spread spectrum on the LVDS and control outputs. The serial link inputs and the LVDS output meet ISO 10605 and IEC 61000-4-2 ESD standards. The deserializer's core supply is 3.3V and the I/O supply is 1.8V to 3.3V. The device is available in a 48-pin TQFP package with an exposed pad and is specified over the -40°C to +105°C automotive temperature range.

II. Manufacturing Information

A. Description/Function:	HDPCP Gigabit Multimedia Serial Link Deserializer with LVDS System Interface
B. Process:	0.18 μ m CMOS
C. Number of Device Transistors:	689613
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea
F. Date of Initial Production:	March 25, 2011

III. Packaging Information

A. Package Type:	48-pin TQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% Matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4228
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	$^{\circ}$ C/W
K. Single Layer Theta Jc:	$^{\circ}$ C/W
L. Multi Layer Theta Ja:	27.6 $^{\circ}$ C/W
M. Multi Layer Theta Jc:	2 $^{\circ}$ C/W

IV. Die Information

A. Dimensions:	166.14X167.32 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal 2-5 = 0.28 / Metal6 = 0.44 micron (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal 2-5 = 0.28 / Metal6 = 0.46 micron (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125 biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 2454 \times 138 \times 2} \text{ (Chi square value for MTTF upper limit)}$$

(where 2454 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 14.1 \times 10^{-9}$$

$$\lambda = 14.1 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the Process results in a FIT Rate of 0.7 @ 25C and 12.3 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lots QR6ZBQ002B, D/C 1131; QR6ZBQ001A, D/C 1109; QR6ZAQ001A, D/C 1030)

The HS69 die type has been found to have all pins able to withstand a transient pulse of:

- ESD-HBM: +/- 4000V all pins per JEDEC JESD22-A114, +/- 8000V CML/LVDS pins to AGND
- ESD-CDM: +/- 750V per JEDEC JESD22-C101
- ESD-MM: +/- 150V per JEDEC JESD22-A115
- ESD gun (contact): +/- 8kV CML/LVDS pins per ISO10605, +/- 10kV CML and +/-8kV LVDS pins per IEC61000-4-2
- ESD gun (air gap): +/- 15kV CML and +/- 30kV LVDS pins per ISO10605, +/- 12kV CML and +/- 20kV LVDS pins per IEC61000-4-2

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78 (lot QR6ZBQ002B, D/C 1131).

Table 1
Reliability Evaluation Test Results

MAX9266GCM/V+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 125	DC Parameters	48	0	QR6ZBQ001A, D/C 1109
	Biased	& functionality	90	0	QR6ZBQ002B, D/C 1131
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.