

RELIABILITY REPORT  
FOR  
MAX9257AGTL/V+ / MAX9257AGCM/V+  
PLASTIC ENCAPSULATED DEVICES

January 24, 2012

**MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX9257AGTL/V+ / MAX9257AGCM/V+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX9257A serializer pairs with the MAX9258A deserializer to form a complete digital video serial link. The MAX9257A/MAX9258A feature programmable parallel data width, parallel clock frequency range, spread spectrum, and preemphasis. An integrated control channel transfers data bidirectionally at power-up during video blanking over the same differential pair used for video data. This feature eliminates the need for external CAN or LIN interface for diagnostics or programming. The clock is recovered from input serial data at MAX9258A, hence eliminating the need for an external reference clock. The MAX9257A serializes 10, 12, 14, 16, and 18 bits with the addition of two encoding bits for AC-coupling. The MAX9258A deserializer links with the MAX9257A to deserialize a maximum of 20 (data + encoding) bits per pixel/parallel clock period for a maximum serial-data rate of 840Mbps. The word length can be adjusted to accommodate a higher pixel/parallel clock frequency. The pixel clock can vary from 5MHz to 70MHz, depending on the serial-word length. Enabling parity adds two parity bits to the serial word. The encoding bits reduce ISI and allow AC-coupling. The MAX9258A receives programming instructions from the electronic control unit (ECU) during the control channel and transmits to the MAX9257A over the serial video link. The instructions can program or update the MAX9257A, MAX9258A, or an external peripheral device, such as a camera. The MAX9257A communicates with the peripheral device with I<sup>2</sup>C or UART. The MAX9257A/MAX9258A operate from a +3.3V core supply and feature separate supplies for interfacing to +1.8V to +3.3V logic levels. These devices are available in 40-lead TQFN or 48-pin LQFP packages. These devices are specified over the -40°C to +105°C temperature range.

**II. Manufacturing Information**

A. Description/Function:	Programmable Serializer/Deserializer with UART/I <sup>2</sup> C Control Channel	
B. Process:	TS35	
C. Number of Device Transistors:	87692	
D. Fabrication Location:	Taiwan	
E. Assembly Location:	China and Thailand	Korea and Malaysia
F. Date of Initial Production:	June 21, 2011	

**III. Packaging Information**

A. Package Type:	40-pin TQFN 5x5	48-pin LQFP 7x7
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2810	#05-9000-2924
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	45°C/W	°C/W
K. Single Layer Theta Jc:	2°C/W	°C/W
L. Multi Layer Theta Ja:	28°C/W	46°C/W
M. Multi Layer Theta Jc:	2°C/W	10°C/W

**IV. Die Information**

A. Dimensions:	117 X 117 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2-4 = 0.6 micron (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2-3 = 0.5 / Metal4 = 0.6 micron (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

**V. Quality Assurance Information**

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

**VI. Reliability Evaluation**

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 170 \times 2} \text{ (Chi square value for MTTF upper limit)}$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 6.47 \times 10^{-9}$$

$$\lambda = 6.47 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the Process results in a FIT Rate of 0.11 @ 25C and 1.80 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The HS42 die type has been found to have all pins able to withstand a transient pulse of:

- ESD-HBM: +/- 3000 per JEDEC JESD22-A114 (lot QGFZFQ001F, D/C 1123)
- ESD-CDM: +/- 750V per JEDEC JESD22-C101 (lot QGFZFQ001F, D/C 1123)
- ESD-MM: +/- 250V per JEDEC JESD22-A115 (lot QGFZFQ001F, D/C 1123)
- ESD gun (contact): +/- 10kV LVDS pins per ISO10605, +/-8kV LVDS pins per IEC61000-4-2
- ESD gun (air gap): +/- 30kV LVDS pins per ISO10605, +/- 20kV LVDS pins per IEC61000-4-2

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78 (lot QGFZFQ001E, D/C 1119).

**Table 1**  
Reliability Evaluation Test Results  
**MAX9257AGTL/V+ / MAX9257ACGM/V+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135C	DC Parameters	90	0	QGFZFQ001F, D/C 1123
	Biased	& functionality	32	0	QGFZEQ001B, D/C 0823
	Time = 192 hrs.		48	0	QGFZCQ001E, D/C 0742

Note 1: Life Test Data may represent plastic DIP qualification lots.