RELIABILITY REPORT

FOR

MAX9244EUM

PLASTIC ENCAPSULATED DEVICES

August 15, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX9244 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9244 deserialize sthree LVDS serial-data inputs into 21 single-ended LVCMOS/ LVTTL outputs. A separate parallel-rate LVDS clock provides the timing for deserialization. The MAX9244 features spread-spectrum capability, allowing the output data and clock frequency to spread over a specified range to reduce EMI. The single-ended data and clock outputs are programmable for a frequency spread of ±2%, ±4%, or no spread. The spread-spectrum function is also available when the MAX9244 operates in non-DC-balanced mode. The modulation rate of the spread is 32kHz for a 33MHz LVDS clock input and scales linearly with frequency. The single-ended outputs have a separate supply, allowing +1.8V to +5V output logic levels.

The MAX9244 features programmable DC balance, allowing isolation between a serializer and deserializer using AC-coupling. The MAX9244 operates with the MAX9209/ MAX9213 serializers and are available with a falling-edge strobe. The LVDS inputs meet ISO 10605 ESD specifications with ±30kV Air-Gap Discharge and ±6kV Contact Discharge ratings.

The MAX9244 is available in a 48-pin TSSOP package and operates over the -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
(All voltages referenced to GND.)	
VCC, LVDSVCC, PLLVCC	-0.5V to +4.0V
VCCO	-0.5V to +6.0V
RxIN_, RxCLKIN_	-0.5V to +4.0V
PWRDWN	-0.5V to +6.0V
SSG, DCB	-0.5V to (VCC + 0.5V)
RxOUT_, RxCLKOUT	-0.5V to (VCCO + 0.5V)
Continuous Power Dissipation (TA = +70°C)	
48-Pin TSSOP (derate 16mW/°C above +70°C)	1282mW
ESD Protection	
Human Body Model (RD = 1.5kΩ, CS = 100pF)	
All Pins to GND	±2.5kV
IEC 61000-4-2 (RD = 330Ω, CS = 150pF)	
LVDS Inputs to GND (Air-Gap Discharge)	±15kV
LVDS Inputs to GND (Contact Discharge)	±8kV
ISO 10605 (RD = 2.0kΩ, CS = 330pF)	
LVDS Inputs to GND (Air-Gap Discharge)	±30kV
LVDS Inputs to GND (Contact Discharge)	±6kV
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	21-Bit Deserializers with Programmable Spread Spectrum and DC Balance
B. Process:	TC35
C. Number of Device Transistors:	65,535
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines, and USA
F. Date of Initial Production:	April, 2005

III. Packaging Information

A. Package Type:	**48-Pin TSSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-2212
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 3

IV. Die Information

A. Dimensions:	108 x 159 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1 = 0.5 / Metal 2 = 0.6 / Metal 3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1 = 0.45 / Metal 2 = 0.5 / Metal 3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.74 \times 10^{-9}$

λ = 13.74 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6150) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the TC35 Process results in a FIT Rate of 0.28 @ 25C and 4.76 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The HS39-1 die type has been found to have all pins able to withstand a transient pulse of ±2500V Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX9244EUM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

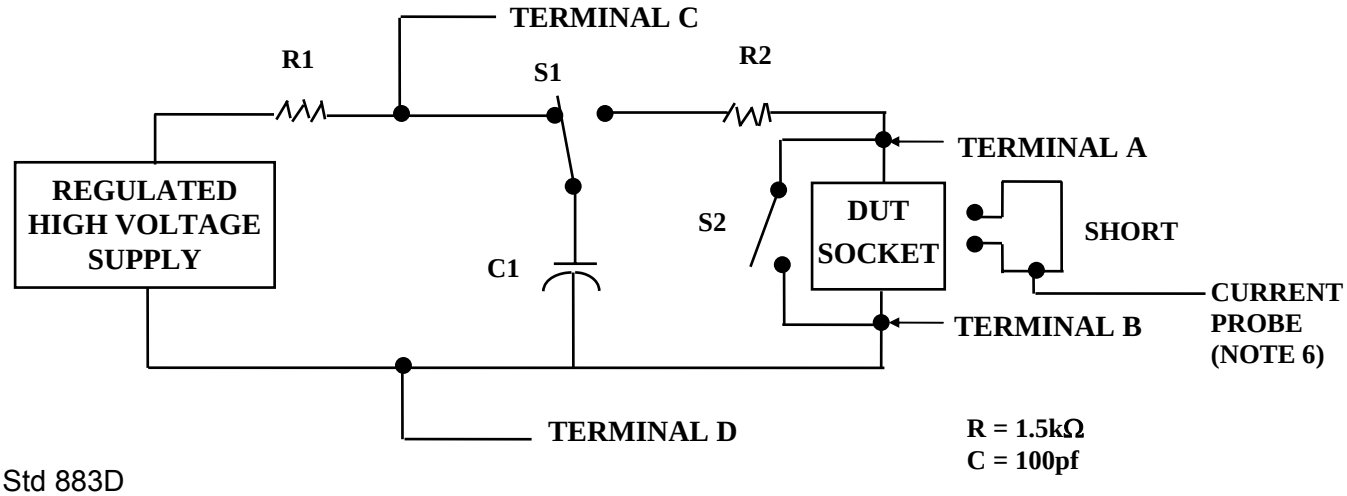
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

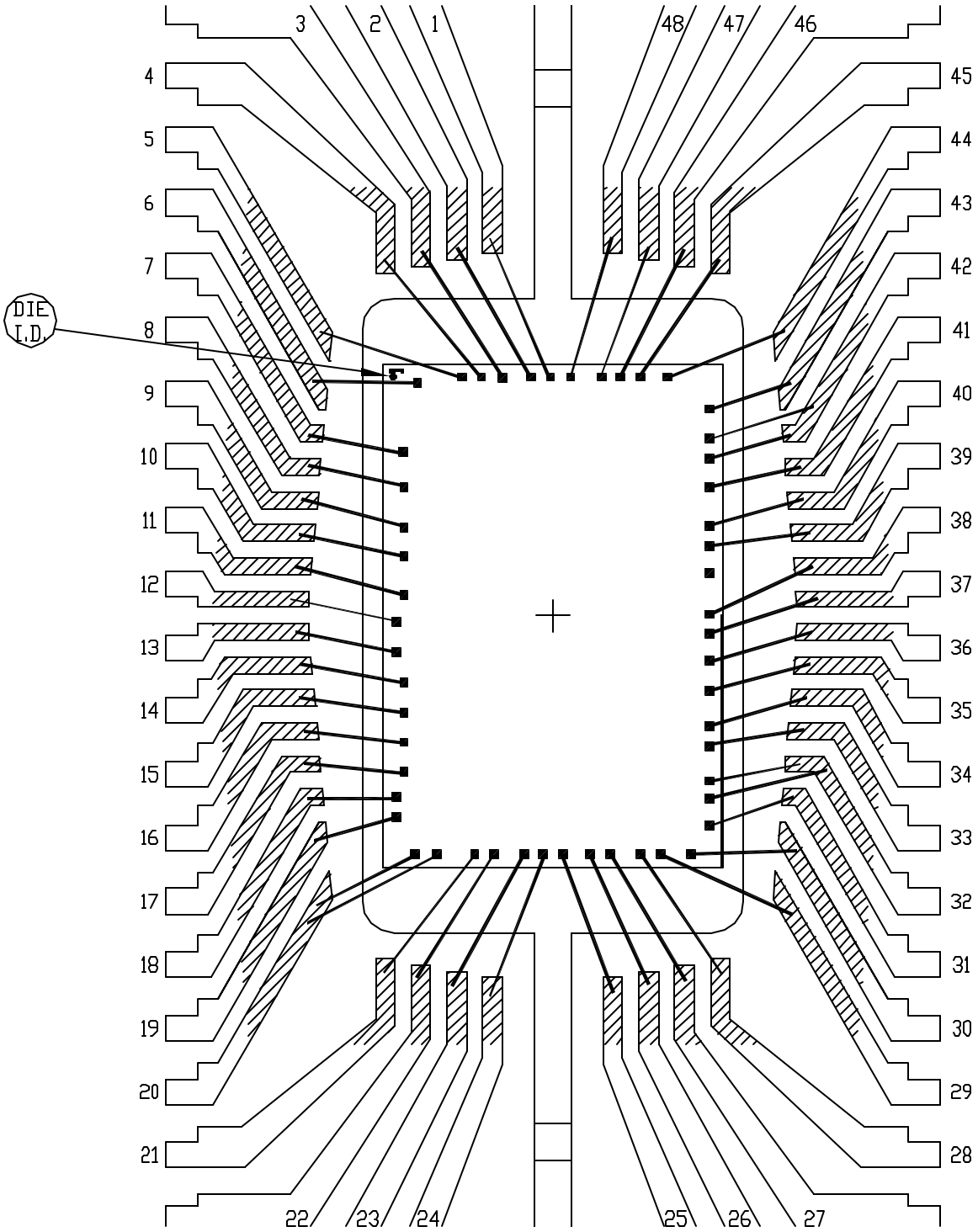
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



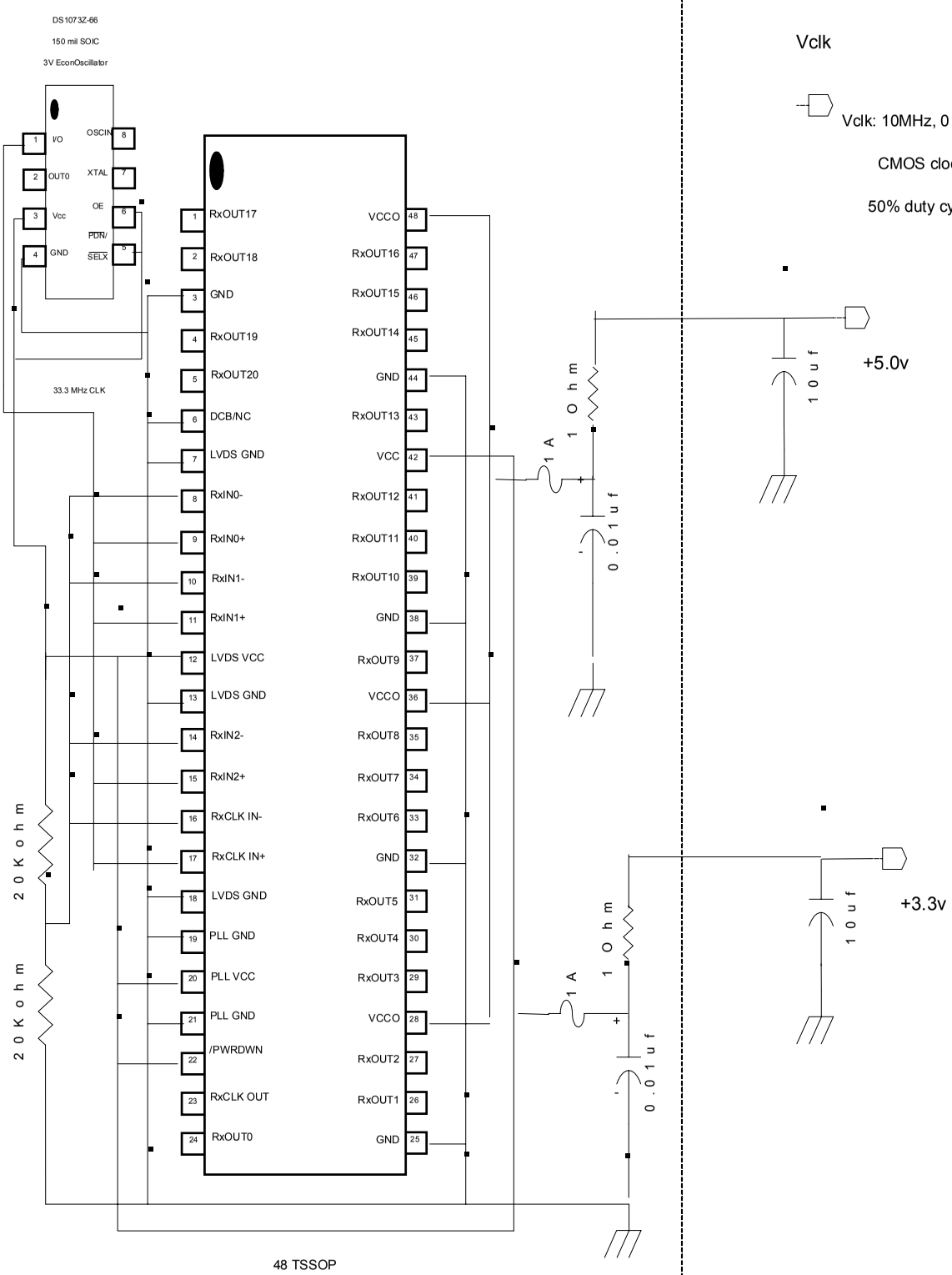
BONDABLE AREA

PKG. CODE: U48-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x197	PKG.			BOND DIAGRAM #: 05-9000-2212	REV: A
	DESIGN				

Burn-In Schematic

ONCE PER SOCKET

ONCE PER BOARD



Vclk

Vclk: 10MHz, 0 to 3.3v

CMOS clock

50% duty cycle

DEVICES: MAX9214/9230/9234/9236/9238/9254/9242/9244/9246

MAX. EXPECTED CURRENT = 150mA **Oven Temperature not exceeding 115C**

TYP. EXPECTED CURRENT = 100mA

TITLE: BI Circuit:MAX9214 (HS31) MAX9230 (HS38) MAX9234/9236/9238 (HS37) MAX9254 (HS60) MAX9242/9244/9246 (HT39)

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