RELIABILITY REPORT

FOR

MAX9240GTM+T

PLASTIC ENCAPSULATED DEVICES

August 30, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX9240GTM+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9240 compact deserializer is designed to interface with a GMSL serializer over 50 coax or 100 shielded twisted-pair (STP) cable. The device pairs with the MAX9271 or MAX9273 serializers. The parallel output is programmable for single or double output. Double output strobes out half of a parallel word on each pixel clock cycle. Double output can be used with GMSL serializers that have the double-input feature. The device features an embedded control channel that operates at 9.6kbps to 1Mbps. Using the control channel, a microcontroller (µC) can program the serializer/deserializer and peripheral device registers at any time, independent of video timing. Two programmable GPIO ports and a continuously sampled GPI input are available. For use with longer cables, the device has a programmable equalizer. Programmable spread spectrum is available on the parallel output. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V and the I/O supply range is 1.7V to 3.6V. The device is available in a 48-pin (7mm x 7mm) TQFN-EP package with 0.5mm lead pitch and operates over the -40°C to +105°C temperature range.

II. Manufacturing Information

A. Description/Function:	6.25MHz to 100MHz, 25-Bit GMSL Deserializer for Coax or STP Cable with Line Fault Detect
B. Process:	TS18
C. Number of Device Transistors:	370041
D. Fabrication Location:	Taiwan
E. Assembly Location:	Taiwan, China, or Thailand
F. Date of Initial Production:	March 27, 2013

III. Packaging Information

A. Package Type:	48-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4846
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	0.8°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	0.8°C/W

IV. Die Information

A. Dimensions:	125.985X125.985 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 78 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.1 \times 10^{-9}$

$\lambda = 14.1$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (ESD lot QAFZ5Q003A D/C 1316, Latch-Up lot QAFZ5Q001E D/C 1251)

The HS50-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of+/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX9240GTM+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	78	0	QAFZ5Q001B, D/C 1216

Note 1: Life Test Data may represent plastic DIP qualification lots.