

RELIABILITY REPORT
FOR
MAX9181EXT+
PLASTIC ENCAPSULATED DEVICES

January 27, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX9181EXT+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	IV.Die Information
.....Attachments	

I. Device Description

A. General

The MAX9181 is an LVPECL-to-LVDS level translator that accepts a single LVPECL input and translates it to a single LVDS output. It is ideal for interfacing between LVPECL and LVDS interfaces in systems that require minimum jitter, noise, power, and space.

Ultra-low, 23psP-P added deterministic jitter and 0.6psRMS added random jitter ensure reliable communication in high-speed links that are highly sensitive to timing errors, especially those incorporating clock-and-data recovery, PLLs, serializers, or deserializers. The MAX9181's switching performance guarantees a 400Mbps data rate, but minimizes radiated noise by guaranteeing 0.5ns minimum output transition time.

The MAX9181 operates from a single 3.3V supply and consumes only 10mA supply current over a -40°C to +85°C temperature range. It is available in a tiny 6-pin SC70 package (half the size of a SOT23). Refer to the MAX9180 data sheet for a low-jitter, low-noise LVDS repeater in an SC70 package.

II. Manufacturing Information

A. Description/Function:	Low-Jitter, Low-Noise LVPECL-to-LVDS Level Translator in an SC70 Package
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Thailand
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	6-pin SC70
B. Lead Frame:	Alloy 42
C. Lead Finish:	NiPdAu Plate
D. Die Attach:	Non Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2801-0029
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	326°C/W
K. Single Layer Theta Jc:	115°C/W

IV. Die Information

A. Dimensions:	32 X 31 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 79 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.6 \times 10^{-9}$$

$\lambda = 13.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HS15-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-200 mA.

Table 1
Reliability Evaluation Test Results

MAX9181EXT+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data