RELIABILITY REPORT

FOR

MAX9173EUE+

PLASTIC ENCAPSULATED DEVICES

January 30, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX9173EUE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9173 quad low-voltage differential signaling (LVDS) line receiver is ideal for applications requiring high data rates, low power, and low noise. The MAX9173 is guaranteed to receive data at speeds up to 500Mbps (250MHz) over controlled-impedance media of approximately 100 . The transmission media can be printed circuit (PC) board traces or cables. The MAX9173 accepts four LVDS differential inputs and translates them to LVCMOS/LVTTL outputs. The MAX9173 inputs are high impedance and require an external termination resistor when used in a point-to-point connection. The device supports a wide common-mode input range of 0.05V to VCC - 0.05V, allowing for ground potential differences and common-mode noise between the driver and the receiver. A fail-safe feature sets the output high when the inputs are open, or when the inputs are undriven and shorted or undriven and parallel terminated. The EN and EN-bar inputs control the high-impedance outputs. The enables are common to all four receivers. Inputs conform to the ANSI TIA/EIA-644 LVDS standard. The flow-through pinout simplifies board layout and reduces crosstalk by separating the LVDS inputs and LVCMOS/LVTTL outputs. The MAX9173 operates from a single 3.3V supply, and is specified for operation from -40°C to +85°C. Refer to the MAX9121/MAX9122 data sheet for lower jitter quad LVDS receivers with parallel fail-safe. Refer to the MAX9123 data sheet for a quad LVDS line driver with flow-through pinout. The device is available in 16-pin TSSOP, SO, and space-saving thin QFN packages.

II. Manufacturing Information

A. Description/Function:	Quad LVDS Line Receiver with Flow-Through Pinout and "In-Path" Fail-Safe
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Philippines
F. Date of Initial Production:	October 25, 2002

III. Packaging Information

A. Package Type:	16-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0197
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	106°C/W
K. Single Layer Theta Jc:	27°C/W
L. Multi Layer Theta Ja:	90°C/W
M. Multi Layer Theta Jc:	27°C/W

IV. Die Information

A. Dimensions:	43X61 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35um
F. Minimum Metal Spacing:	0.35um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.80 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot QAN0AQ001C, D/C 0232)

The HS24 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1

Reliability Evaluation Test Results

MAX9173EUE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0	QAN0AQ001C, D/C 0232

Note 1: Life Test Data may represent plastic DIP qualification lots.