

RELIABILITY REPORT
FOR
MAX9158EGM
PLASTIC ENCAPSULATED DEVICES

March 5, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX9158 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX9158 is a quad bus LVDS (BLVDS) transceiver for heavily loaded, half-duplex multipoint buses. A 44-lead QFN package and flow-through pinout allow the transceiver to be placed near the connector. The MAX9158 drives LVDS levels into a 27 Ω load (double terminated, heavily loaded LVDS bus) at up to 200Mbps. An input fail-safe circuit ensures the receiver output is high when the differential inputs are open, or undriven and shorted, or undriven and terminated. The MAX9158 operates from a single 3.3V supply, consuming 77mA supply current with drivers enabled, and 19.9mA with drivers disabled.

The MAX9158's high-impedance I/Os (except for receiver outputs) when $V_{CC} = 0V$ or open, combined with glitch-free power-up and power-down, allow hot swapping of cards in multicard bus systems; 7.3pF (max) BLVDS I/O capacitance minimizes bus loading.

The MAX9158 is offered in a 7mm x 7mm 44-lead QFN package, and is fully specified for the -40°C to +85°C extended temperature range.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VCC, AVCC to GND	-0.3V to +4.0V
DO_+/RIN_+, DO_-/RIN_- to GND	-0.3V to +4.0V
DIN_, DE_, RE_ to GND	-0.3V to +4.0V
RO_ to GND	-0.3V to (VCC + 0.3V)
AGND to GND	-0.3V to +0.3V
Short-Circuit Duration (DO_+/RIN_+, DO_-/RIN_-)	Continuous
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
ESD Protection Human Body Model (DO_+/RIN_+, DO_-/RIN_-)	±4kV
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
44-Pin QFN	2105mW
Derates above +70°C	
44-Pin QFN	24.3mW/°C

II. Manufacturing Information

A. Description/Function:	Quad Bus LVDS Transceiver in 44 QFN
B. Process:	TC35
C. Number of Device Transistors:	1796
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	April, 2002

III. Packaging Information

A. Package Type:	44-Pin QFN
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-2801-0038
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	100 x 68 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9}$$

$$\lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5898) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The HS16-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$ per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX9158EGM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

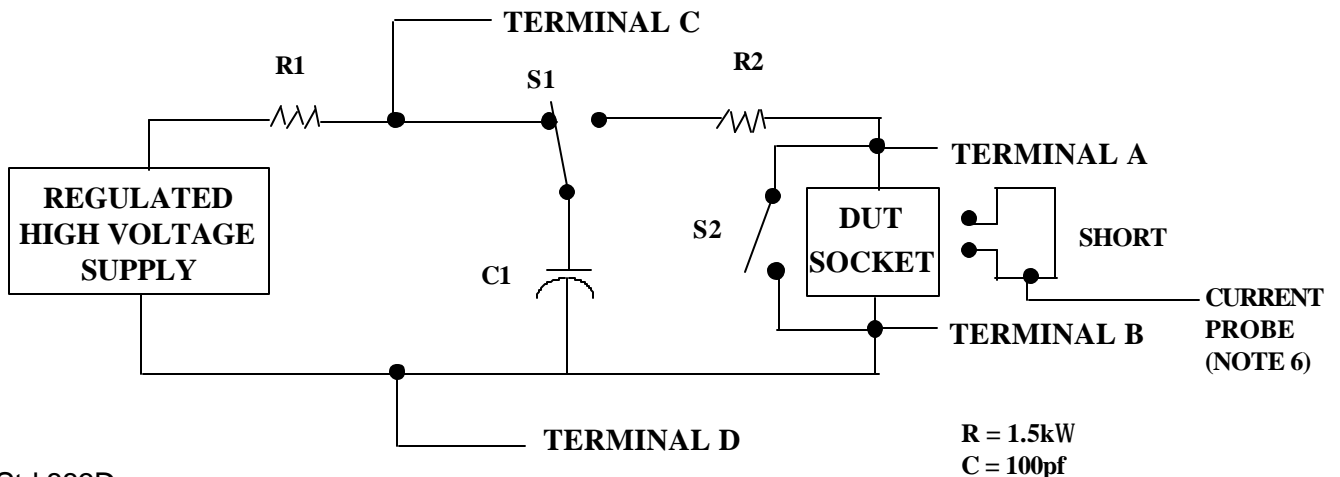
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

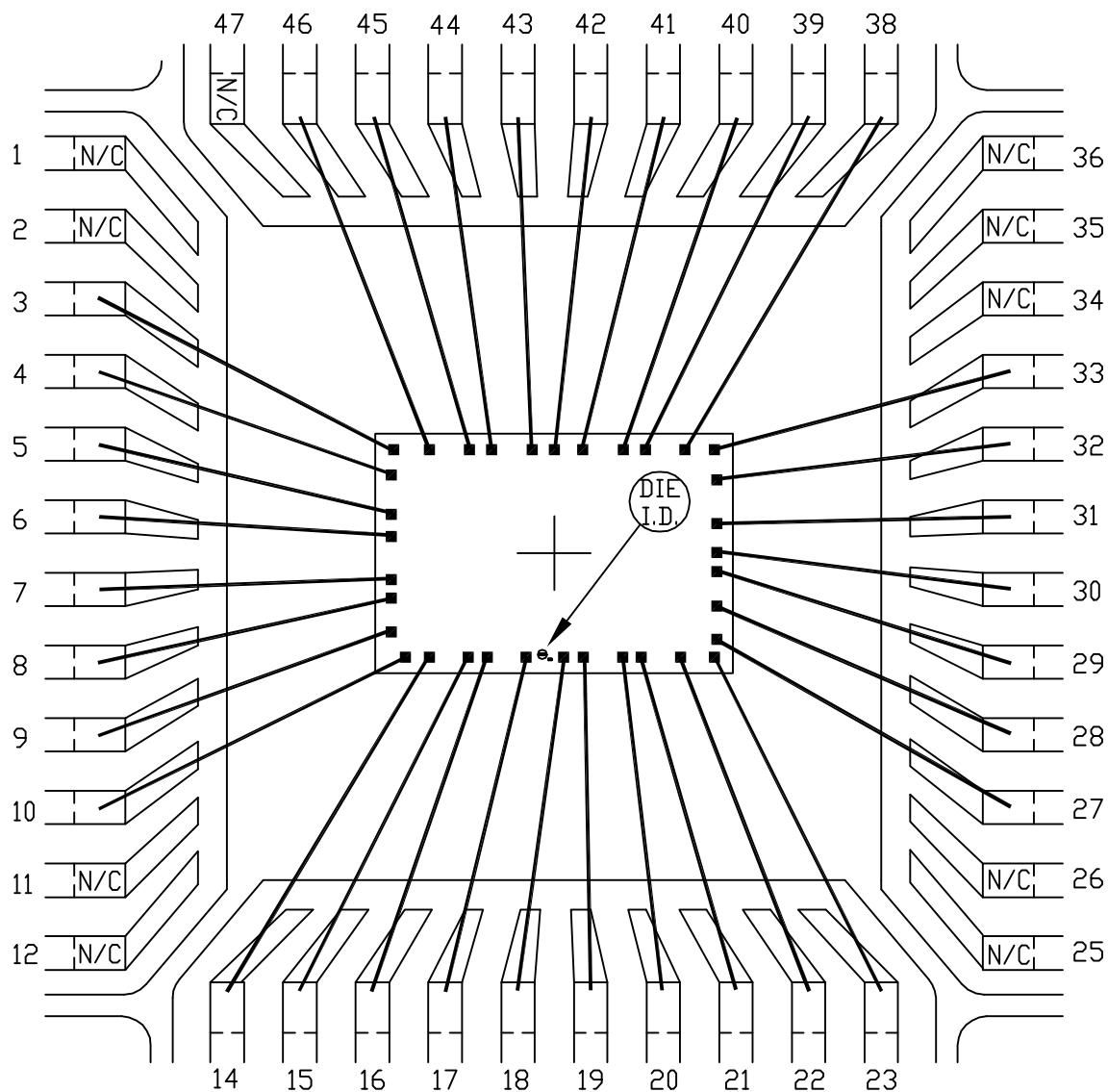
3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



7x7x0.8 MM QFN THIN PKG.

EXPOSED PAD PKG.



DEPOPULATED PINS: 13, 24, 37 & 48.

PKG. CODE: T4877-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 177x177	PKG. DESIGN			BOND DIAGRAM #: 05-2801-0038	REV: C

