RELIABILITY REPORT

FOR

MAX9125ESE+

PLASTIC ENCAPSULATED DEVICES

November 9, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Don Lipps
Quality Assurance
Manager, Reliability Engineering

Conclusion

The MAX9125ESE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX9125/MAX9126 quad low-voltage differential signaling (LVDS) line receivers are ideal for applications requiring high data rates, low power, and reduced noise. The MAX9125/MAX9126 are guaranteed to receive data at speeds up to 500Mbps (250MHz) over controlled-impedance media of approximately 100 . The transmission media may be printed circuit (PC) board traces or cables. The MAX9125/MAX9126 accept four LVDS differential inputs and translate them to 3.3V CMOS outputs. The MAX9126 features integrated parallel termination resistors (nominally 115), which eliminate the requirement for four discrete termination resistors and reduce stub length. The MAX9125 inputs are high impedance and require an external termination resistor when used in a point-to-point connection. The devices support a wide common-mode input range of 0.05V to 2.35V, allowing for ground potential differences and common-mode noise between the driver and the receiver. A fail-safe feature sets the output high when the inputs are open, or when the inputs are undriven and shorted or parallel terminated. The EN and EN-bar inputs control the high-impedance output and are common to all four receivers. Inputs conform to the ANSI TIA/EIA-644 LVDS standard. The MAX9125/ MAX9126 operate from a single +3.3V supply, are specified for operation from -40°C to +85°C, and are available in 16-pin TSSOP and SO packages. Refer to the MAX9124 data sheet for a quad LVDS line driver.

II. Manufacturing Information

A. Description/Function:	Quad LVDS Line Receivers with Integrated Termination
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	January 26, 2001

III. Packaging Information

A. Package Type:	16-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2801-0014
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	82.2°C/W
M. Multi Layer Theta Jc:	32°C/W

IV. Die Information

A. Dimensions:	52 X 60 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm F.
Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 70 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 15.7 \times 10^{-9}$

λ = 15.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot Q1S0BQ001C, D/C 0111)

The HS12 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX9125ESE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	70	0	Q1S0BQ001D, DC 0111

Note 1: Life Test Data may represent plastic DIP qualification lots.