

RELIABILITY REPORT  
FOR  
MAX9122ESE+  
(MAX9121/MAX9122)  
PLASTIC ENCAPSULATED DEVICES

March 19, 2009

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

<b>Approved by</b>
Ken Wendel
Quality Assurance
Director, Reliability Engineering

## Conclusion

The MAX9122ESE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

<b>I. ....Device Description</b>	<b>V. ....Quality Assurance Information</b>
<b>II. ....Manufacturing Information</b>	<b>VI. ....Reliability Evaluation</b>
<b>III. ....Packaging Information</b>	<b>IV. ....Die Information</b>
<b>.....Attachments</b>	

### I. Device Description

#### A. General

The MAX9121/MAX9122 quad low-voltage differential signaling (LVDS) differential line receivers are ideal for applications requiring high data rates, low power, and low noise. The MAX9121/MAX9122 are guaranteed to receive data at speeds up to 500Mbps (250MHz) over controlled-impedance media of approximately 100 . The transmission media may be printed circuit (PC) board traces or cables. The MAX9121/MAX9122 accept four LVDS differential inputs and translate them to LVCMOS outputs. The MAX9122 features integrated parallel termination resistors (nominally 107 ), which eliminate the requirement for four discrete termination resistors and reduce stub lengths. The MAX9121 inputs are high impedance and require an external termination resistor when used in a point-to-point connection. The devices support a wide common-mode input range of 0.05V to 2.35V, allowing for ground potential differences and common-mode noise between the driver and the receiver. A fail-safe feature sets the output high when the inputs are open, or when the inputs are undriven and shorted or parallel terminated. The EN and active-low EN inputs control the high-impedance output. The enables are common to all four receivers. Inputs conform to the ANSI TIA/EIA-644 LVDS standard. Flow-through pinout simplifies PC board layout and reduces crosstalk by separating the LVDS inputs and LVCMOS outputs. The MAX9121/MAX9122 operate from a single +3.3V supply, and are specified for operation from -40°C to +85°C. These devices are available in 16-pin TSSOP and SO packages. Refer to the MAX9123 data sheet for a quad LVDS line driver with flow-through pinout.

## II. Manufacturing Information

A. Description/Function:	Quad LVDS Line Receivers with Integrated Termination and Flow-Through Pinout
B. Process:	0.35UM 2 Poly 3 Metal CMOS (TS352P3M)
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Carsem Malaysia, Hana Thailand, ATP Philippines, Unisem Malaysia
F. Date of Initial Production:	January 26, 2001

## III. Packaging Information

A. Package Type:	16-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	82.2°C/W
K. Multi Layer Theta Jc:	32°C/W

## IV. Die Information

A. Dimensions:	45 X 61 mils
B. Passivation:	Silicon Dioxide/Silicon Nitride
C. Interconnect:	Al/Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35 um
F. Minimum Metal Spacing:	0.35 um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	Silicon Dioxide
I. Die Separation Method:	Saw

## V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.4 \times 10^{-9}$$

$$\lambda = 13.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the TS352P3M Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

### C. E.S.D. and Latch-Up Testing

The HS08-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX9122ESE+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
<b>Moisture Testing</b> (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data