

RELIABILITY REPORT
FOR
MAX907xxA
PLASTIC ENCAPSULATED DEVICES

February 19, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX907 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	
IV.Die InformationAttachments

I. Device Description

A. General

The MAX907 dual, high-speed, ultra-low-power voltage comparator is designed for use in systems powered from a single +5V supply. Its 40ns propagation delay (with 5mV input overdrive) is achieved with a power consumption of only 3.5mW per comparator. The wide input common-mode range extends from 200mV below ground to within 1.5V of the positive supply rail.

Because it is micropower, high-speed comparators that operate from a single +5V supply and include built-in hysteresis, this device replaces a variety of older comparators in a wide range of applications.

The MAX907 outputs are TTL-compatible, requiring no external pullup circuitry. All inputs and outputs can be continuously shorted to either supply rail without damage. This easy-to-use comparator incorporates internal hysteresis to ensure clean output switching even when the devices are driven by a slow-moving input signal.

The dual MAX907 is available in 8-pin DIP and SO packages. This comparator is ideal for single +5V-supply applications that require the combination of high speed, precision, and ultra-low power dissipation.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Positive Supply Voltage (V+ to GND)	+6V
Differential Input Voltage	-0.3V to (V+ + 0.3V)
Common-Mode Input Voltage	-0.3V to (V+ + 0.3V)
Input/Output Short-Circuit Duration to V+ or GND	Continuous
Operating Temperature Ranges:	
MAX907C_ _	0°C to +70°C
MAX907E_ _	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin SO	471mW
8-Pin DIP	727mW
Derates above +70°C	
8-Pin SO	5.88mW/°C
8-Pin DIP	9.09mW/°C

II. Manufacturing Information

A. Description:	Dual, High-Speed, Ultra-Low-Power, Single-Supply TTL Comparators
B. Process:	CB3
C. Number of Device Transistors:	262
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines or Thailand
F. Date of Initial Production:	March, 1993

III. Packaging Information

A. Package Type:	8-Pin PDIP	8-Pin SO
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1501-0255	Buildsheet # 05-1501-0254
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	80 x 24 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Gold
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1: 1.4 microns Metal 2: 1.4 microns Metal 3: 3 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1: 1.6 microns Metal 2: 1.6 microns Metal 3: 3 microns (as drawn)
G. Bondpad Dimensions:	2.7 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 79 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.75 \times 10^{-9} \quad \lambda = 13.75 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0002) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The CM73 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX907xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		79	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	DIP SO	77 77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

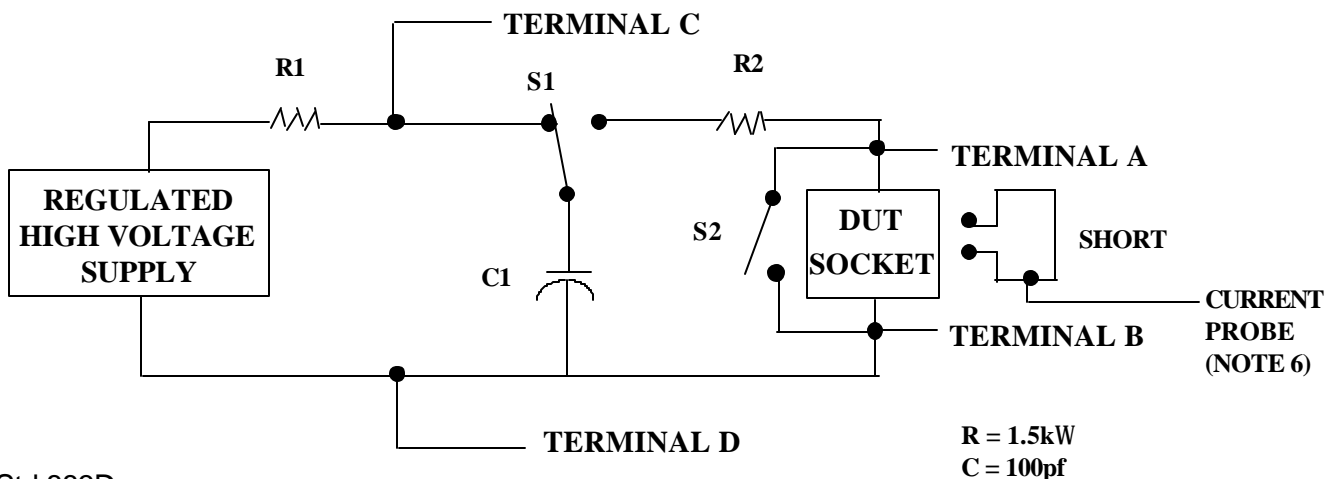
2/ No connects are not to be tested.

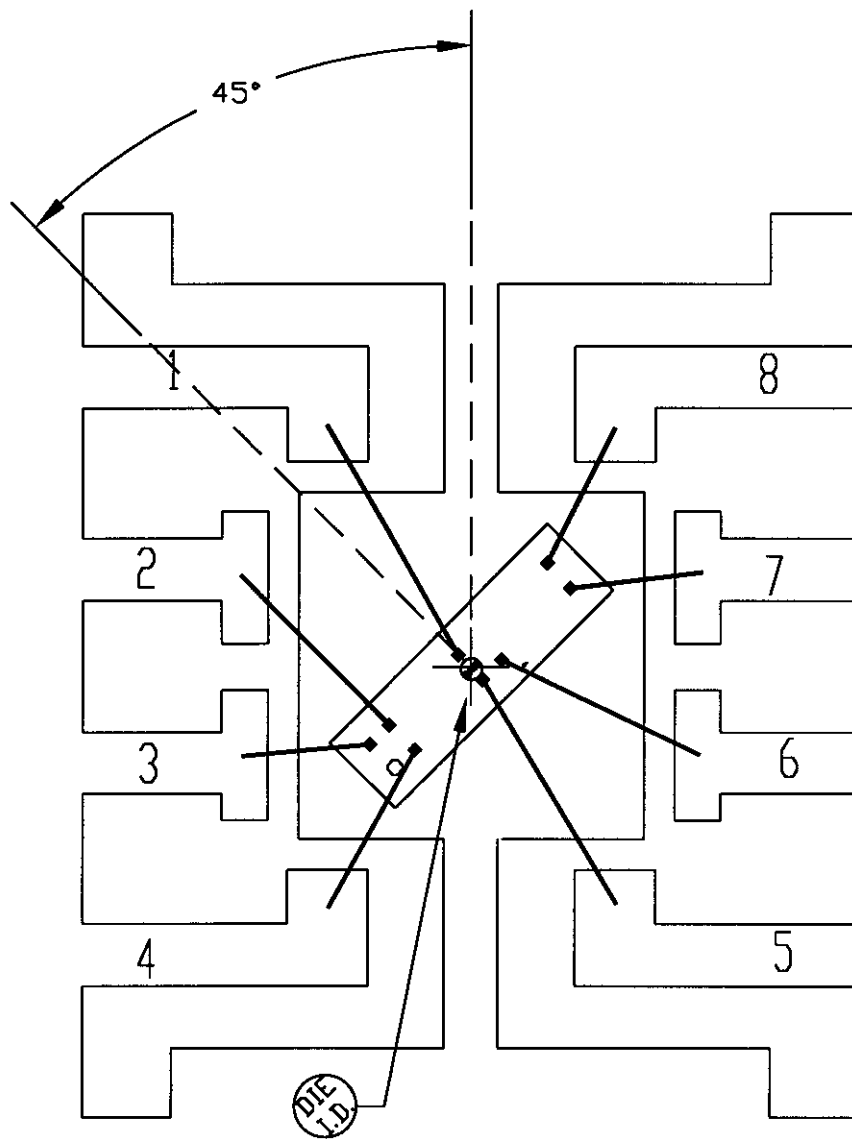
3/ Repeat pin combination 1 for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND , $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE:

S8-2

SIGNATURES

DATE

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CAV./PAD SIZE:

90 X 90

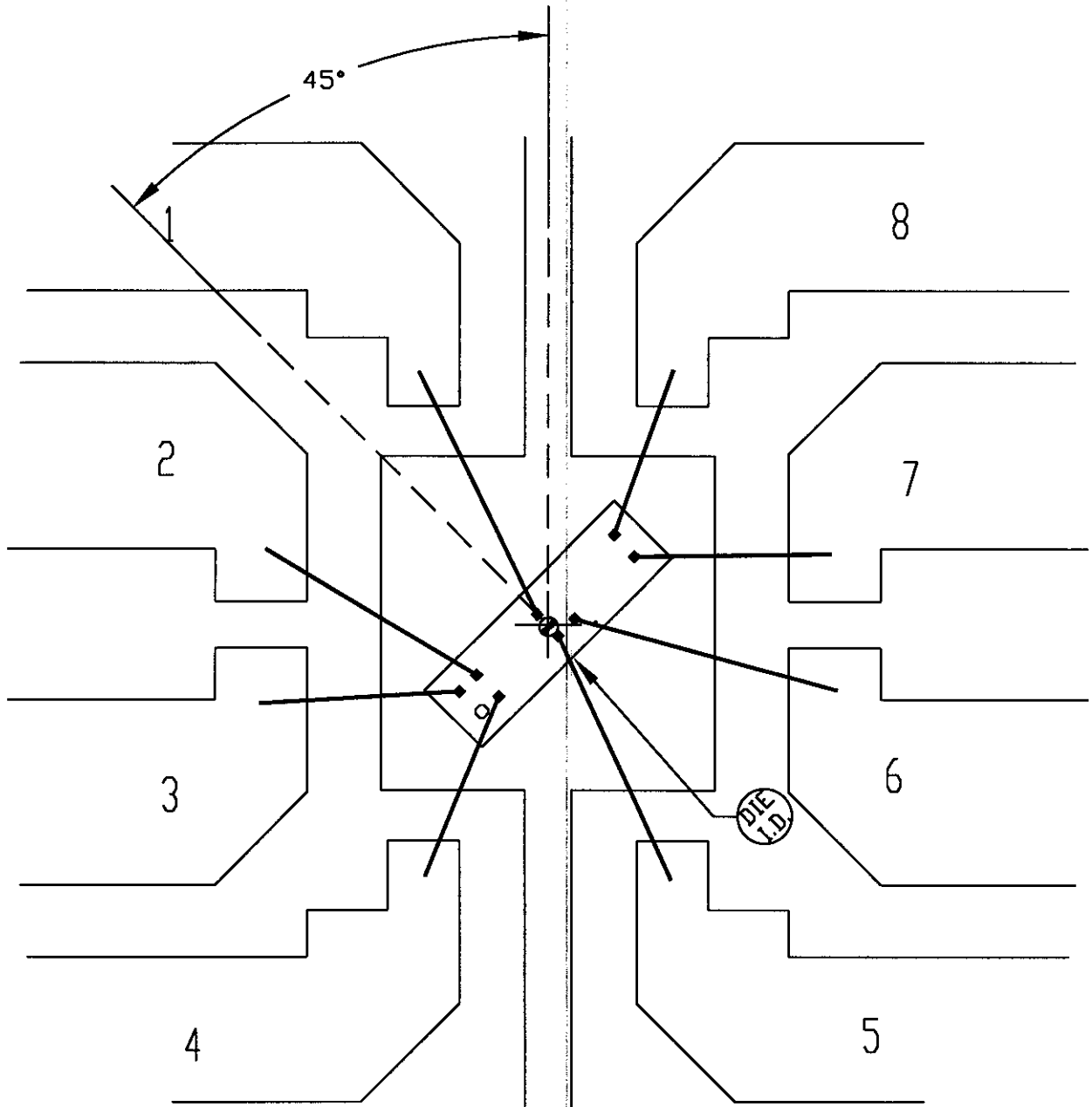
PKG.
DESIGN

BOND DIAGRAM #:

05-1501-0254

REV:

A



PKG. CODE: P8-1

SIGNATURES

DATE

MAXIM
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CAV./PAD SIZE: 100 X 100

PKG.
DESIGN

BOND DIAGRAM #: 05-1501-0255

REV: A

