

RELIABILITY REPORT
FOR
MAX892LEUA+
PLASTIC ENCAPSULATED DEVICES

April 23, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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| Approved by |
| Sokhom Chum |
| Quality Assurance |
| Reliability Engineer |

Conclusion

The MAX892LEUA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description**A. General**

The MAX891L/MAX892L smart, low-voltage, P-channel, MOSFET power switches are intended for high-side load-switching applications. These switches operate with inputs from 2.7V to 5.5V, making them ideal for both 3V and 5V systems. Internal current-limiting circuitry protects the input supply against overload. Thermal-overload protection limits power dissipation and junction temperatures. The MAX891L/MAX892L's maximum current limits are 500mA and 250mA, respectively. The current limit through the switch is programmed with a resistor from SET to ground. When the switch is on, the quiescent supply current is a low 13 μ A. When the switch is off, the quiescent current decreases to 0.1 μ A. The MAX891L/MAX892L are available in 8-pin μ MAX® packages.

II. Manufacturing Information

| | |
|----------------------------------|---|
| A. Description/Function: | Current-Limited, High-Side P-Channel Switches with Thermal Shutdown |
| B. Process: | B12 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | Oregon |
| E. Assembly Location: | Philippines, Thailand, Malaysia |
| F. Date of Initial Production: | Pre 1997 |

III. Packaging Information

| | |
|--|--------------------------|
| A. Package Type: | 8-pin uMAX |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-1701-0300 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | 1 |
| J. Single Layer Theta Ja: | 221°C/W |
| K. Single Layer Theta Jc: | 42°C/W |
| L. Multi Layer Theta Ja: | 206.3°C/W |
| M. Multi Layer Theta Jc: | 42°C/W |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 84 X 60 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 1.2 microns (as drawn) |
| F. Minimum Metal Spacing: | 1.2 microns (as drawn) |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 6.9 \times 10^{-9}$$

$$\lambda = 6.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the B12 Process results in a FIT Rate of 0.02 @ 25C and 0.33 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot NNUEGA017B D/C 0313, Latch-Up lot SNUEHQ001A D/C 0340)

The PW77-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX892LEUA+

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|----------------------------------|-----------------|------------------------|-------------|--------------------|----------------------|
| Static Life Test (Note 1) | Ta = 135°C | DC Parameters | 80 | 0 | INUDEQ001F, D/C 9937 |
| | Biased | & functionality | 80 | 0 | NNUEDQ002B, D/C 9845 |
| | Time = 192 hrs. | | | | |

Note 1: Life Test Data may represent plastic DIP qualification lots.