

RELIABILITY REPORT
FOR
MAX8893CEWV+T
PLASTIC ENCAPSULATED DEVICES

June 1, 2012

MAXIM INTEGRATED PRODUCTS

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Approved by
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Quality Assurance
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Conclusion

The MAX8893CEWV+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	IV.Die Information
II.Manufacturing Information	V.Quality Assurance Information
III.Packaging Information	VI.Reliability Evaluation
.....Attachments	

I. Device Description

A. General

The MAX8893A/MAX8893B/MAX8893C power-management integrated circuits (PMICs) are designed for a variety of portable devices including cellular handsets. The PMICs include a high-efficiency step-down DC-DC converter, five low-dropout linear regulators (LDOs) with programmable output voltages, individual power-on/off control inputs, a load switch, and a USB high-speed switch. These devices maintain high efficiency with a low no-load supply current, and the small 3.0mm x 2.5mm WLP package makes them ideal for portable devices. The step-down DC-DC converter utilizes a proprietary 4MHz hysteretic PWM control scheme that allows for ultra-small external components. Internal synchronous rectification improves efficiency and eliminates the external Schottky diode that is required in conventional step-down converters. Its output voltage is programmable by the I²C serial interface and output current is guaranteed up to 500mA. LDO1, LDO4, and LDO5 offer low 45 μ V_{RMS} output noise and low dropout of only 100mV at 100mA. They deliver up to 300mA, 150mA, and 200mA continuous output currents, respectively. LDO2 and LDO3 each deliver 300mA continuous output current with very low ground current. All LDO output voltages are programmable by the I²C serial interface. Three standard versions of the PMIC are available with different LDO default startup voltages (see Table 1 in the full data sheet). The MAX8893A/MAX8893B/MAX8893C are available in a 3.0mm x 2.5mm, 30-bump WLP package.

II. Manufacturing Information

A. Description/Function:	µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP
B. Process:	S4
C. Number of Device Transistors:	25860
D. Fabrication Location:	Texas or Japan
E. Assembly Location:	Texas
F. Date of Initial Production:	11/20/2009

III. Packaging Information

A. Package Type:	30 bmp 5x6 WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4000 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	41°C/W
L. Multi Layer Theta Ja:	N/A
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	100 X 120 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{281 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 15.6 \times 10^{-9}$$

$$\lambda = 15.6 \text{ F.I.T. (60\% confidence level @ 25}^\circ\text{C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TXGZAQ001D D/C 0950)

The PR48 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX8893CEWV+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 281 hrs.	DC Parameters & functionality	48	0	TXGZAQ001D, D/C 0950

Note 1: Life Test Data may represent plastic DIP qualification lots.