

RELIABILITY REPORT  
FOR  
**MAX8887EZKxx**  
PLASTIC ENCAPSULATED DEVICES

March 30, 2004

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX8887 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX8887 low-dropout linear regulator operates from a 2.5V to 5.5V input and delivers up to 300mA continuous (500mA pulsed) current. The MAX8887 is optimized for low-noise operation. The MAX8887 includes an open-drain POK output flag. The regulator features exceptionally low 100mV dropout at 200mA. This device is available in a variety of preset output voltages in the 1.5V to 3.3V range.

An internal PMOS pass transistor allows the low 55 $\mu$ A supply current to remain independent of load, making this device ideal for portable battery-powered equipment such as personal digital assistants (PDAs), cellular phones, cordless phones, and notebook computers. Other features include a micropower shutdown mode, short-circuit protection, thermal shutdown protection, and an active-low open-drain power-OK (POK) output that indicates when the output is out of regulation.

The MAX8887 is available in a thin 5-pin SOT23 package that is only 1mm high.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN, /SHDN, POK to GND	-0.3V to +6.0V
OUT, BP to GND	-0.3V to + (VIN 0.3V)
Output Short-Circuit Current Duration	Continuous
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
5-Pin SOT23	727mW
Derates above +70°C	
5-Pin SOT	23 9.1mW/°C

## II. Manufacturing Information

- A. Description/Function: Low-Dropout, 300mA Linear Regulator
- B. Process: B8 (Standard 0.8 micron silicon gate CMOS)
- C. Number of Device Transistors: 620
- D. Fabrication Location: California, USA
- E. Assembly Location: Philippines
- F. Date of Initial Production: December, 2000

## III. Packaging Information

- A. Package Type: **5-Pin SOT23**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate or 100% Matte Tin
- D. Die Attach: Silver-Filled Epoxy
- E. Bondwire: Gold (1.0 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-2301-0084
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020A: Level 1

## IV. Die Information

- A. Dimensions: 59 x 40 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 0.8 microns (as drawn)
- F. Minimum Metal Spacing: 0.8 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{SiO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲  
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9}$$

$$\lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5302) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The PY90 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500\text{V}$  Human Body Model (HBM), per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit),  $\pm 300\text{V}$  Machine Model (MM) per JEDEC JESD22-A115-A and  $\pm 1000\text{V}$  Charge Device Model (CDM) per JEDEC JESD22-C101-A. Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX887EUKxx**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

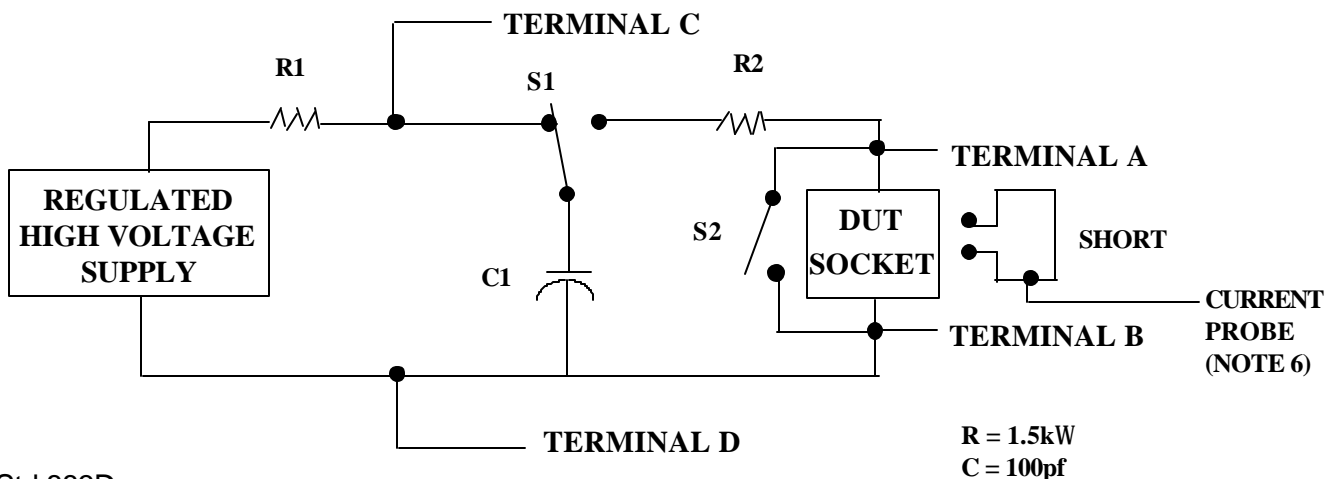
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

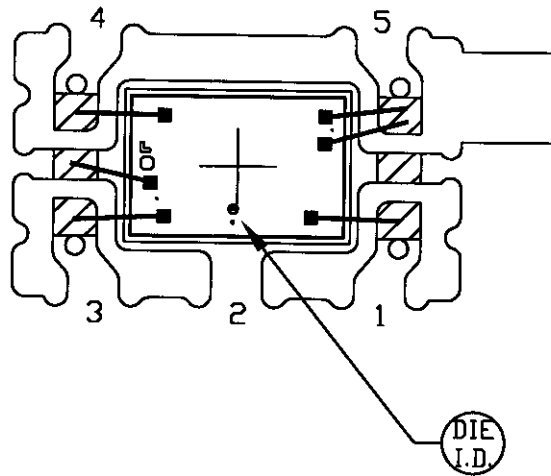
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



THIN SOT PACKAGE



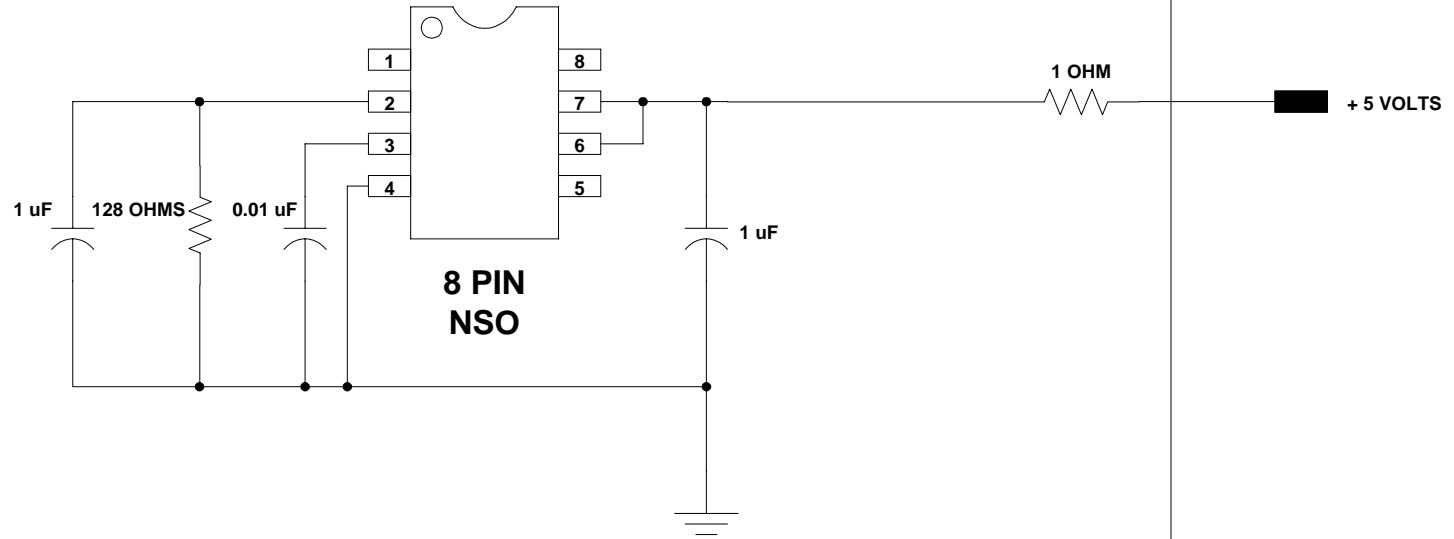
CAVITY DOWN

 BONDABLE AREA

PKG. CODE: Z5-1		SIGNATURES _	DATE	<b>MAXIM</b> CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 63x44	PKG. DESIGN			BOND DIAGRAM #: 05-2301-0084	REV: B

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 8877 / 8878 / 1872 / 8887 / 8888

MAX. EXPECTED CURRENT = 20mA