RELIABILITY REPORT

FOR

MAX8855ETJ+

PLASTIC ENCAPSULATED DEVICES

June 25, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX8855ETJ+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX8855 high-efficiency, dual step-down regulator is capable of delivering up to 5A at each output. The device operates from a 2.35V to 3.6V supply, and provides output voltages from 0.6V to 0.9 x VIN, making it ideal for on-board point-of-load applications. Total output error is less than ±1% over load, line, and temperature. The MAX8855 operates in PWM mode with a switching frequency ranging from 0.5MHz to 2MHz, set by an external resistor. It can also be synchronized to an external clock in the same frequency range. Two internal switching regulators operate 180° out-of-phase to reduce the input ripple current, and consequently reduce the required input capacitance. The high operating frequency minimizes the size of external components. High efficiency, internal dual-nMOS design keeps the board cool under heavy loads. The voltage-mode control architecture and the high-bandwidth (> 15MHz typ) voltage-error amplifier allow a type III compensation scheme to be utilized to achieve fast response under both line and load transients, and also allow for ceramic output capacitors. Programmable soft-start reduces input inrush current. Two enable inputs allow the turning on/off of each output individually, resulting in great flexibility for systemlevel designs. A reference input is provided to facilitate output-voltage tracking applications. The MAX8855 is available in a 32-pin thin QFN (5mm x 5mm) package with 0.8mm max height.

II. Manufacturing Information

A. Description/Function:	Dual, 5A, 2MHz Step-Down Regulator
B. Process:	S4
C. Number of Device Transistors:	13556
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	July 28, 2007

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2046
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	1.7°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	1.7°C/W

IV. Die Information

A. Dimensions:	78 X 120 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4 Process results in a FIT Rate of 4.6 @ 25C and 79.2 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PP35 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX8855ETJ+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data