

RELIABILITY REPORT  
FOR  
MAX8791BGTA+  
PLASTIC ENCAPSULATED DEVICES

November 4, 2014

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

<b>Approved by</b>
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Quality Assurance
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## Conclusion

The MAX8791BGTA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX8791/MAX8791B are single-phase, synchronous, noninverting MOSFET drivers. The MAX8791/MAX8791B are intended to work with controller ICs like the MAX8736 or MAX8786, in multiphase notebook CPU core regulators. The regulators can either step down directly from the battery voltage to create the core voltage, or step down from the main system supply. The single-stage conversion method allows the highest possible efficiency, while the 2-stage conversion at higher switching frequency provides the minimum possible physical size. The low-side drivers are optimized to drive 3nF capacitive loads with 4ns/8ns typical fall/rise times, and the high-side driver with 8ns/10ns typical fall/rise times. Adaptive dead-time control prevents shoot-through currents and maximizes converter efficiency. The MAX8791/MAX8791B are available in a small, lead-free, 8-pin, 3mm x 3mm TQFN package.

## II. Manufacturing Information

A. Description/Function:	Single-Phase, Synchronous MOSFET Drivers
B. Process:	S45
C. Number of Device Transistors:	1168
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	October 21, 2006

## III. Packaging Information

A. Package Type:	8-pin TQFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2360
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	42°C/W
M. Multi Layer Theta Jc:	8.3°C/W

## IV. Die Information

A. Dimensions:	42X48 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.04 @ 25C and 0.69 @ 55C (0.8 eV, 60% UCL).

### B. E.S.D. and Latch-Up Testing (lot TV63AQ001D, D/C 0941)

The PE10-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX8791BGTA+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SV60CZ001C, D/C 0637

Note 1: Life Test Data may represent plastic DIP qualification lots.