MAX8751ETJ
Rev. A

RELIABILITY REPORT

FOR

MAX8751ETJ

PLASTIC ENCAPSULATED DEVICES

April 28, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX8751 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

The MAX8751 cold-cathode-fluorescent lamp (CCFL) inverter controller is designed to drive multiple CCFLs using the fixed-frequency, full-bridge inverter topology. The MAX8751 operates in resonant mode during striking and switches over to constant-frequency operation after all the lamps are lit. This unique feature ensures reliable striking under all conditions and reduces the transformer stress.

The MAX8751 can drive large power MOSFETs typically used in applications where one power stage drives four or more CCFL lamps in parallel. An internal 5.35V linear regulator powers the MOSFET drivers and most of the internal circuitry. The controller operates over a wide input-voltage range (6V to 28V) with high power to light efficiency. The device also includes safety features that effectively protect against many single-point fault conditions, including lamp-out and short-circuit conditions.

The MAX8751 achieves a 10:1 dimming range by "chopping" the lamp current on and off using the digital pulsewidth modulation (DPWM) method. The DPWM frequency can be accurately adjusted with a resistor or synchronized to an external signal. The brightness is controlled by an analog voltage on the CNTL pin.
The MAX8751 is capable of synchronizing and adjusting the phase of the gate drivers and DPWM oscillator. These features allow multiple MAX8751 ICs to be connected in a daisy-chain configuration. The switching frequency and DPWM frequency can be easily adjusted using external resistors, or synchronized with system signals. If the controller loses the external sync signals, it switches over to the internal oscillators and keeps operating. Phase-shift select pins PS1 and PS2 can be used to program up to four different phase shifts, allowing up to five MAX8751s to be used together.

The MAX8751 is available in a low-profile, 32-pin TQFN package and operates over the -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
IN, LX1, LX2 to GND	-0.3V to +30V
BST1, BST2 to GND	-0.3V to +36V
BST2 to LX2	-0.3V to +6V
VCC to GND	-0.3V to +6V
GH1 to LX1	-0.3V to VBST1 + 0.3V
GH2 to LX2	-0.3V to VBST2 + 0.3V
CNTL, SEL COMP, GL1, GL2, DPWM, HF, LF, HFCK, HSYNC, LSYNC, LFCK, PCOMP, PS1, PSCK, TFLT, PS2, SHDN to GND	-0.3V to VCC + 0.3V
IFB, ISEC, VFB to GND	-6V to +6V
PGND1, PGND2 to GND	-0.3V to +3V
Continuous Power Dissipation (TA = +70°C)	
32-Pin TQFN (derate 21.3mW/°C above +70°C)	1702.1mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Fixed-Frequency, Full-Bridge CCFL Inverter Controller
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	7743
D. Fabrication Location:	Texas, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	July, 2005

III. Packaging Information

A. Package Type:	**32-Lead Thin QFN (5x5)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.0 mil dia)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-1831
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity Per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	80 x 93 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1.** Using these results, the Failure Rate (λ) calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 22.91 \times 10^{-9}$ $\lambda = 22.91$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6522) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PD83 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8759ETI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

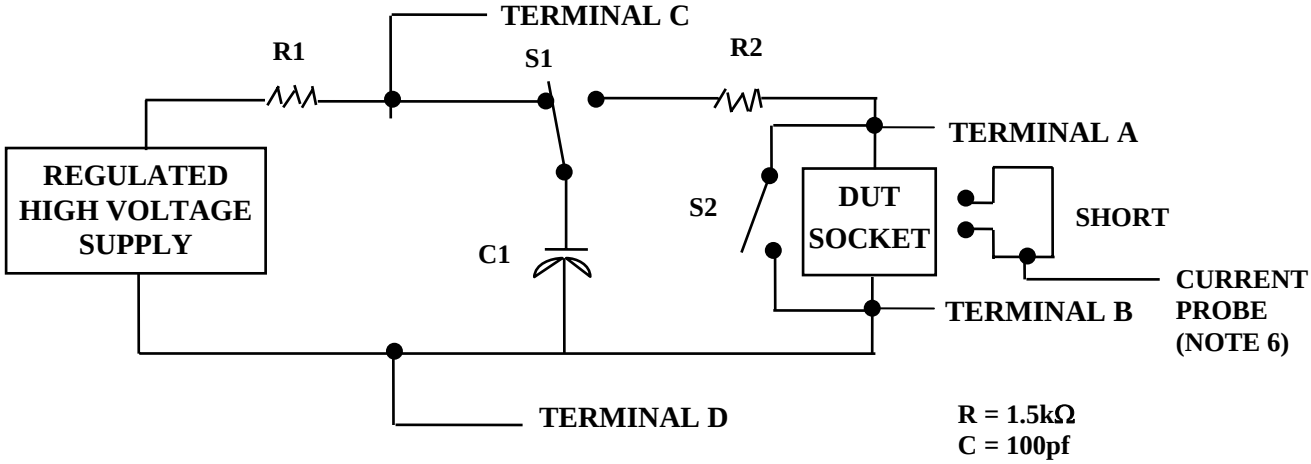
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

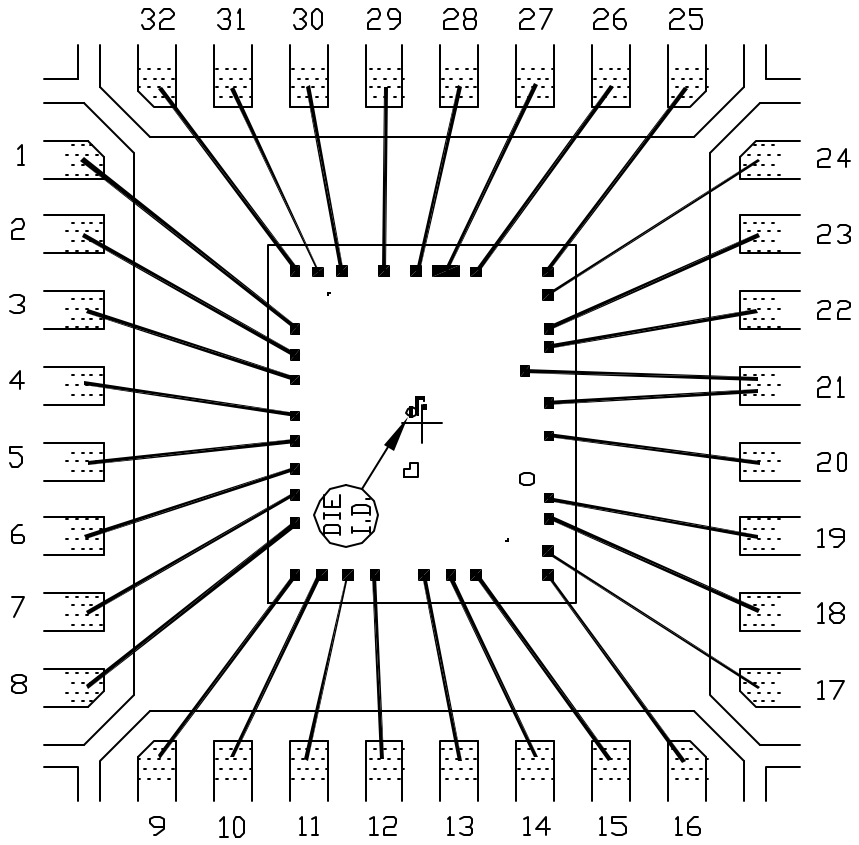
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

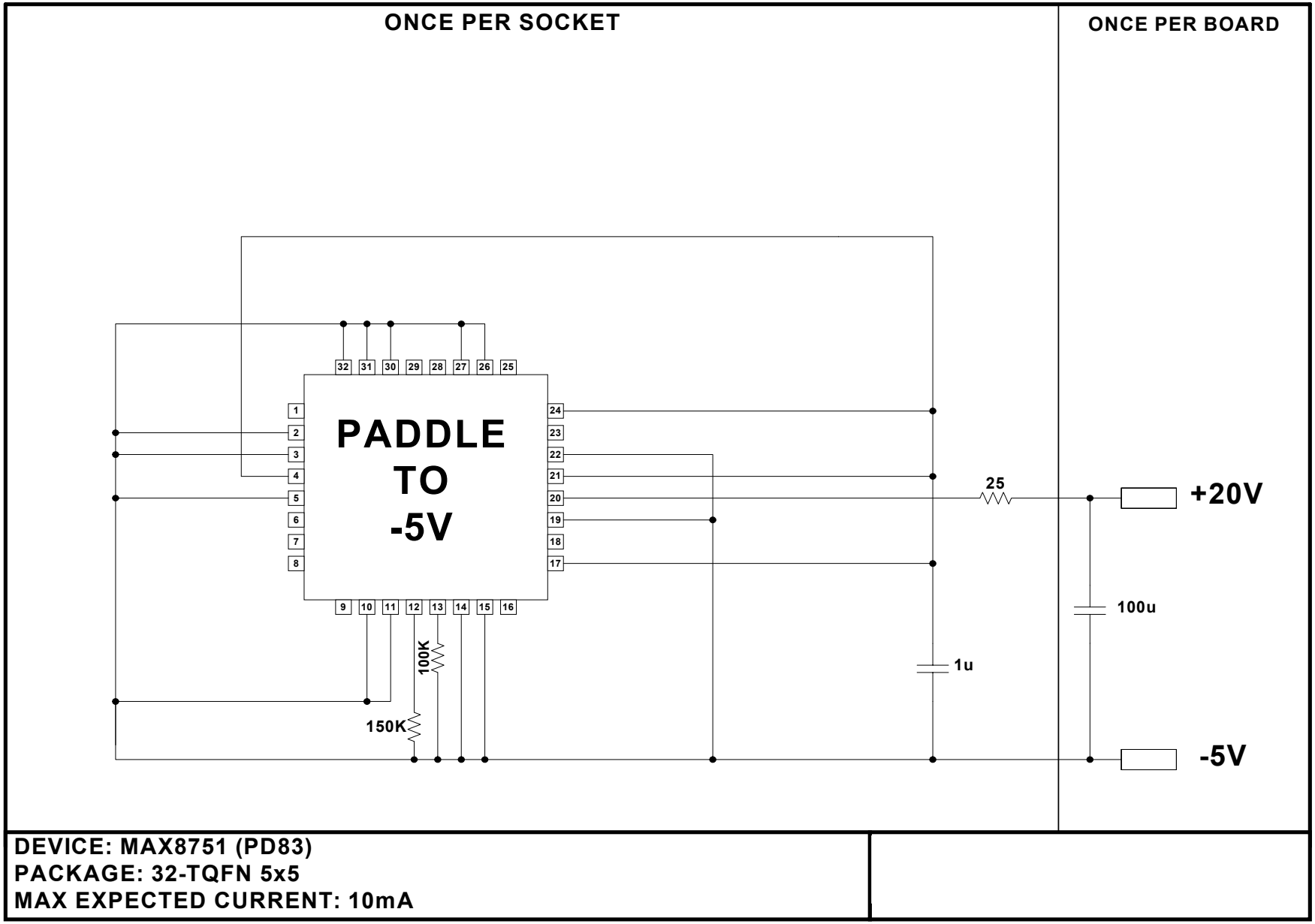


5x5x0.8mm THIN QFN PKG. EXPOSED PAD PKG.



BONDABLE AREA

PKG. CODE: T3255-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 150x150	PKG.			BOND DIAGRAM #: 05-9000-1831	REV: A
	DESIGN				


ONCE PER SOCKET
ONCE PER BOARD
PADDLE
TO
-5V
32 31 30 29 28 27 26 25
1 2 3 4 5 6 7 8
24 23 22 21 20 19 18 17
9 10 11 12 13 14 15 16
25
+20V
100u
100K
1u
150K
-5V
DEVICE: MAX8751 (PD83)
PACKAGE: 32-TQFN 5x5
MAX EXPECTED CURRENT: 10mA