RELIABILITY REPORT

FOR

MAX875xxxA

PLASTIC ENCAPSULATED DEVICES

October 10, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX875 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX875 precision +5V reference offers excellent accuracy and very low power consumption. Extremely low temperature drift combined with excellent line and load regulation permits stable operation over a wide range of electrical and environmental conditions. Low 10Hz to 1kHz noise, typically $30\mu V_{RMS}$, makes this part suitable for 12-bit data-acquisition systems.

A TRIM pin facilitates adjustment of the reference voltage over a 4% range, using only a $100k\Omega$ potentiometer. A voltage output proportional to temperature provides a source for temperature compensation circuits, temperature warning circuits and other applications.

B. Absolute Maximum Ratings

<u>ltem</u>	Rating
V _{CC} to GND V _{OUT} , TRIM, TEMP, TEST Output Short-Circuit Duration (to GND) Current into Any Pin Storage Temp. Lead Temp. (10 sec.)	20V (GND - 0.3V) to (V _{CC} + 0.3V) Continuous ±50mA -65°C to +150°C +300°C
Continuous Power Dissipation (TA = +70°C)	
8-Lead NSO	471mW
8-Lead PDIP	727mW
Derates above +70°C	
8-Lead NSO	5.88mW/°C
8-Lead NSO	9.09mW/°C

II. Manufacturing Information

A. Description/Function: Low-Power, Low-Drift, +5V Precision Voltage Reference

B. Process: BA5 - Standard 24V 5 micron Bipolar Process

C. Number of Device Transistors: 76

D. Fabrication Location: Arizona, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: July, 1992

III. Packaging Information

A. Package Type: 8 Lead NSO 8 Lead PDIP

B. Lead Frame: Copper Copper

C. Lead Finish: Solder Plate Solder Plate

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.) Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-0901-0084 Buildsheet # 05-0901-0082

H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard JESD22-A112: Level 1 Level 1

IV. Die Information

A. Dimensions: 75 x 103 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 5 microns (as drawn)

F. Minimum Metal Spacing: 5 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager-Reliability Operations)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \text{ x } 4389 \text{ x } 460 \text{ x } 2}$$
 (Chi square value for MTTF upper limit)
$$\lambda = 2.36 \text{ x } 10^{-9}$$
 Temperature Acceleration factor assuming an activation energy of 0.8eV
$$\lambda = 2.36 \text{ x } 10^{-9}$$

$$\lambda = 2.36 \text{ F.I.T.}$$
 (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples fom production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0024) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (RR-1M).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RF18-2 die type has been found to have all pins able to withstand a transient pulse of ± 800 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 100 mA and/or ± 20 V.

Table 1 Reliability Evaluation Test Results

MAX875xxxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	(Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		460	0
Moisture Testin	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO PDIP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots. Note 2: Generic Process/Package Data

Attachment #1

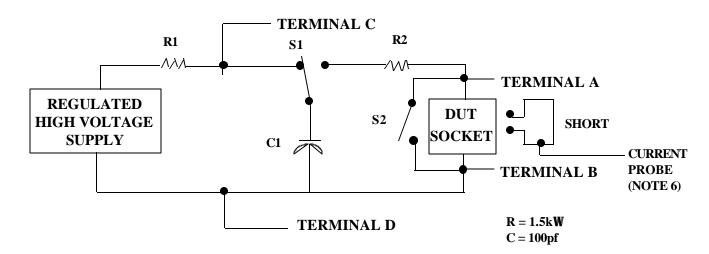
TABLE II. Pin combination to be tested. 1/2/

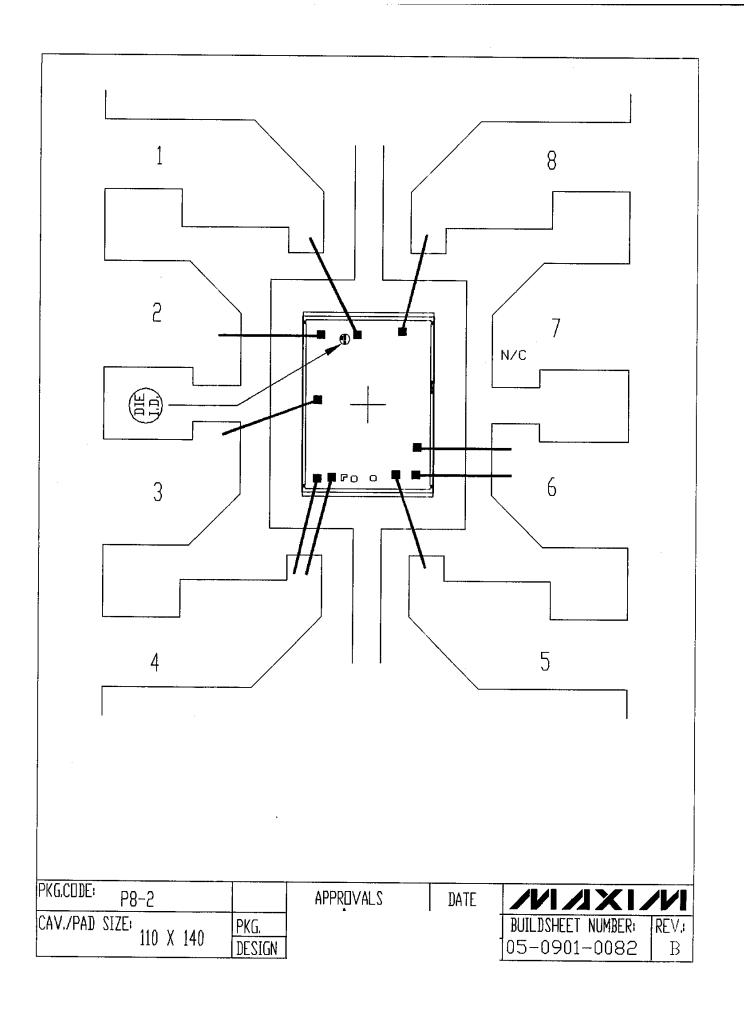
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

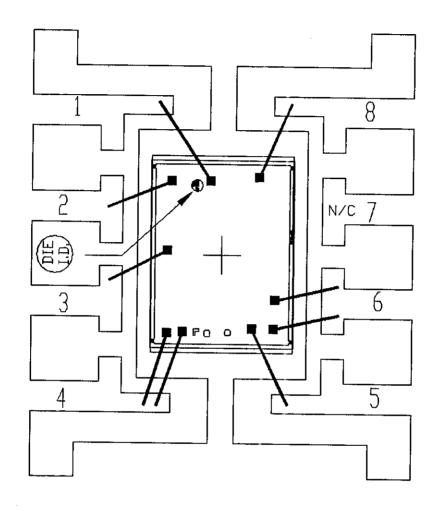
- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- $\underline{3/}$ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







PKG.CODE: S8-4		APPROVALS	DATE	/VI/IXI	///
CAV./PAD SIZE: 90 X 130	PKG.			BUILDSHEET NUMBER:	REV.:
70 X 130	DESIGN			05-0901-0084	B

