RELIABILITY REPORT

FOR

MAX8740ETB+

PLASTIC ENCAPSULATED DEVICES

July 1, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX8740ETB+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX8740 is a high-performance, step-up DC-DC converter that provides a regulated supply voltage for active-matrix, thin-film transistor (TFT), liquid-crystal displays (LCDs). The MAX8740 incorporates currentmode, fixed-frequency, pulse-width modulation (PWM) circuitry with a built-in n-channel power MOSFET to achieve high efficiency and fast transient response. Users can select 640kHz or 1.2MHz operation using a logic input pin (FREQ). The high switching frequencies allow the use of ultra-small inductors and low-ESR ceramic capacitors. The current-mode architecture provides fast transient response to pulsed loads. A compensation pin (COMP) gives users flexibility in adjusting loop dynamics. The 30V internal MOSFET can generate output voltages up to 28V from a 2.6V and 5.5V input voltage range. Soft-start slowly ramps the input current and is programmed with an external capacitor. The MAX8740 is available in a 10-pin thin DFN package.

II. Manufacturing Information

A. Description/Function:	TFT-LCD Step-Up DC-DC Converter
B. Process:	S45
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	China, Malaysia, Philippines, Thailand
F. Date of Initial Production:	April 23, 2005

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1812
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	9°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	9°C/W

IV. Die Information

A. Dimensions:	57 X 87 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 22 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 50 \times 10^{-9}$

λ = 50 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SU00A3001B D/C 0510)

The PD72 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX8740ETB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	22	0	SU00A3001B, D/C 0510

Note 1: Life Test Data may represent plastic DIP qualification lots.