

RELIABILITY REPORT
FOR
MAX8728ETJ+
PLASTIC ENCAPSULATED DEVICES

July 21, 2006

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX8728 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX8728 generates all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in TVs and monitors. It includes step-down and step-up regulators, positive and negative charge pumps, and a dual-mode, logic-controlled, high-voltage switch control block. The MAX8728 can operate from input voltages from 7V to 13.2V and is optimized for LCD TV panel and LCD monitor applications running directly from 12V supplies.

The step-up and step-down regulators feature internal power MOSFETs and high-frequency operation allowing the use of small inductors and capacitors, resulting in a compact solution. Both switching regulators use fixed-frequency, current-mode control architectures, providing fast load-transient response and easy compensation. The positive and negative charge-pump regulators provide TFT gate driver supply voltages. Both output voltages can be adjusted with external resistive voltage-dividers.

The MAX8728 is available in a small (5mm x 5mm), low-profile (0.8mm), 32-pin thin QFN package and operates over the -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN, INL, SUPP to GND	-0.3V to +14V
SUPP to IN	±0.3V
DRVN to GNDP	-0.3V to VSUPP + 0.3V
CTL, EN, SHDN, OUT1, VL, VCC to GND	-0.3V to +6V
COMP, FB1, FB2, FBN, FBP, FSEL, DEL, THR, MODE, REF to GND	-0.3V to VCC + 0.3V
GND1, GND2, GNDP to GND	±0.3V
BST to GND1	-0.3V to +20V
LX1 to BST	-6V to +0.3V
LX2 to GND2	-0.3V to +19V
DRVN, LX1, GATE to GND1	-0.3V to VIN + 0.3V
GON, SRC to GND	-0.3V to +40V
SRC to GON	-0.3V to +40V
SRC to SUPP	-0.3V to +30V
SRC to SUPP (momentary)	-14V to +30V
GON to SUPP	-14V to +30V
SRC to DRN	-0.3V to +40V
DRN to GND	-0.3V to +40V
GON to DRN	-0.3V to +30V
VL Short Circuit to GND	Momentary
REF Short Circuit to GND	Continuous
DRVN RMS Current	-400mA
DRVN RMS Current	+100mA
LX2 RMS Current	+1.6A
GND2 RMS Current	+1.6A
LX1 RMS Current	-1.6A
Continuous Power Dissipation (TA = +70°C)	
32-Pin Thin QFN (derate 34.5mW/°C above +70°C)	2758mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

- A. Description/Function: Low-Cost, Multiple-Output Power Supply for LCD Monitors/TVs
- B. Process: B8 (Standard 0.8 micron silicon gate CMOS)
- C. Number of Device Transistors: 6,752
- D. Fabrication Location: Texas, USA
- E. Assembly Location: Thailand
- F. Date of Initial Production: January, 2006

III. Packaging Information

- A. Package Type: 32-pin TQFN-EP
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate or 100% Matte Tin
- D. Die Attach: Silver-Filled Epoxy
- E. Bondwire: Gold (1.3 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-9000-2202
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

IV. Die Information

- A. Dimensions: 122 x 117 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 0.8 microns (as drawn)
- F. Minimum Metal Spacing: 0.8 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 22.91 \times 10^{-9}$$

$$\lambda = 22.91 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-6433) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PD60 die type has been found to have all pins able to withstand a transient pulse of $\pm 1500\text{V}$, per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX8728ETJ+

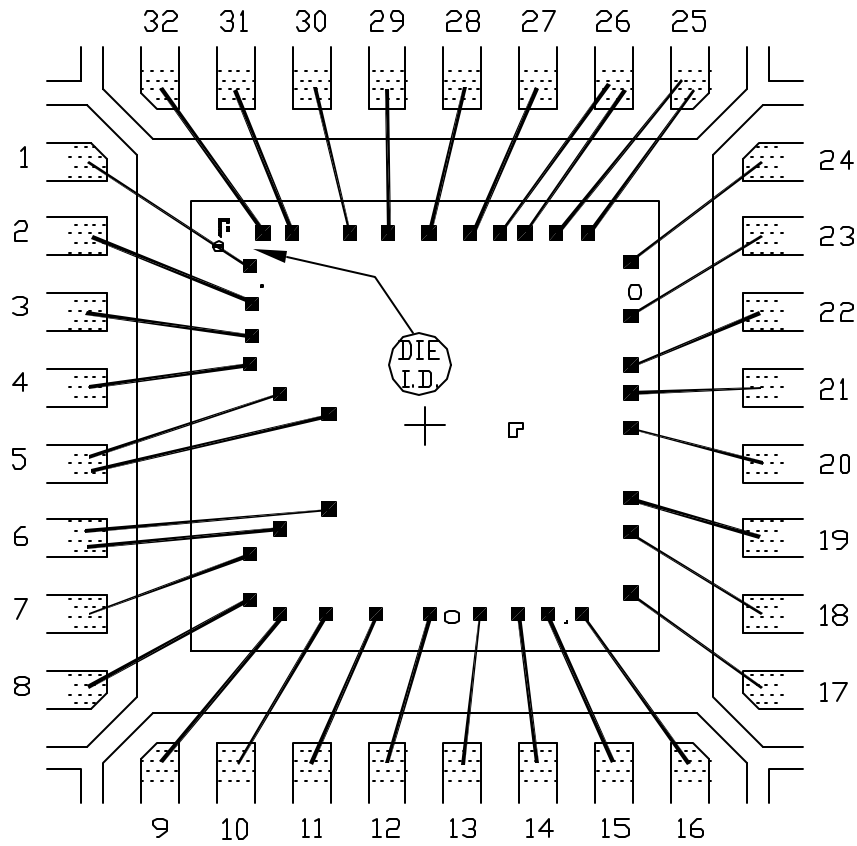
TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TQFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

5x5x0.8mm THIN QFN PKG.

EXPOSED PAD PKG.



 BONDABLE AREA

PKG. CODE: T3255-4		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 150x150	PKG. DESIGN			BOND DIAGRAM #: 05-9000-2202	REV: A

