RELIABILITY REPORT

FOR

MAX8621xETG

PLASTIC ENCAPSULATED DEVICES

August 24, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Conclusion

The MAX8621Y/Z successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8621Y/MAX8621Z power-management integrated circuit (PMICs) is designed for a variety of portable devices including cellular handsets. This PMICs include two high-efficiency step-down DC-DC converters, four low-dropout linear regulators (LDOs) with pin-programmable capability, one open-drain driver, a 60ms (typ) reset timer, and power-on/off control logic. These devices offer high efficiency with a no-load supply current of 160µA, and their small thin QFN 4mm x 4mm package makes them ideal for portable devices.

The step-down DC-DC converter utilizes a proprietary 4MHz hysteretic-PWM control scheme that allows for ultra-small external components. Internal synchronous rectification improves efficiency and eliminates the external Schottky diode that is required in conventional step-down converters. The output voltage is adjustable from 0.6V to 3.3V. The output current is guaranteed up to 500mA.

The four LDOs offer low 45µV_{RMS} output noise and low dropout of only 100mV at 100mA. OUT1 and OUT2 deliver 300mA (min) of continuous output current. OUT3 and OUT4 deliver 150mA (min) of continuous output current. The output voltages are pin selectable by SEL1 and SEL2 for flexibility. The MAX8621Y/MAX8621Z offers different sets of LDO output voltages.

A microprocessor reset output (RESET-bar) monitors OUT1 and warns the system of impending power loss, allowing safe shutdown. RESET-bar asserts during power-up, power-down, shutdown, and fault conditions where V_{OUT1} is below its regulation voltage.

A 200mA driver output is provided to control LED backlighting or provide an open-drain connection for resistors such as in feedback networks.

B. Absolute Maximum Ratings

Item	Rating
PWRON, IN1, IN2, IN3, RESET, FB1, FB2, ENDR, REFBP, SEL1, SEL2 to GND	-0.3V to +6.0V
EN2, EN3, EN4, DR to GND	-0.3V to (VIN3 + 0.3V)
OUT1, OUT2, OUT3, OUT4 to GND	-0.3V to (VIN2 + 0.3V)
PGND1, PGND2 to GND	-0.3V to + 0.3V
LX1, LX2 Current	±1.5ARMS
LX1, LX2 to GND (Note 1)	-0.3V to (VIN1 + 0.3V)
DR Current	0.5ARMS
Continuous Power Dissipation (TA = +70°C) 24-Pin 4mm x 4mm Thin QFN (derate 27.8mW/°C above +70°C)	2222.2mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: LX_ has internal clamp diodes to GND and IN1. Applications that forward-bias these diodes should take care not to exceed the IC's package dissipation limits.

II. Manufacturing Information

A. Description/Function: Dual Step-Down DC-DC Power-Management ICs for Portable Devices

B. Process: B8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 5,850

D. Fabrication Location: California or Texas, USA

E. Assembly Location: Thailand

F. Date of Initial Production: January, 2005

III. Packaging Information

A. Package Type: **24-Pin TQFN**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate or 100% Matte Tin

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (.13 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-9000-1529

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

IV. Die Information

A. Dimensions: 100 x 100

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)

F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.88 \times 10^{-9}$

λ = 22.88 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-6440) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PN96Z-1 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8621xETG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TQFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

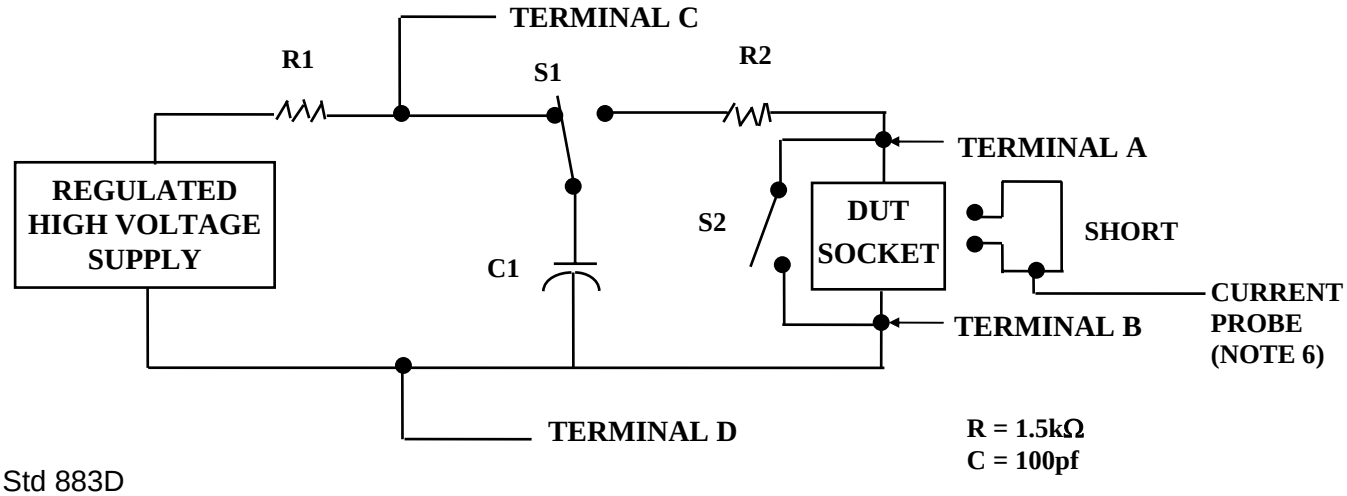
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

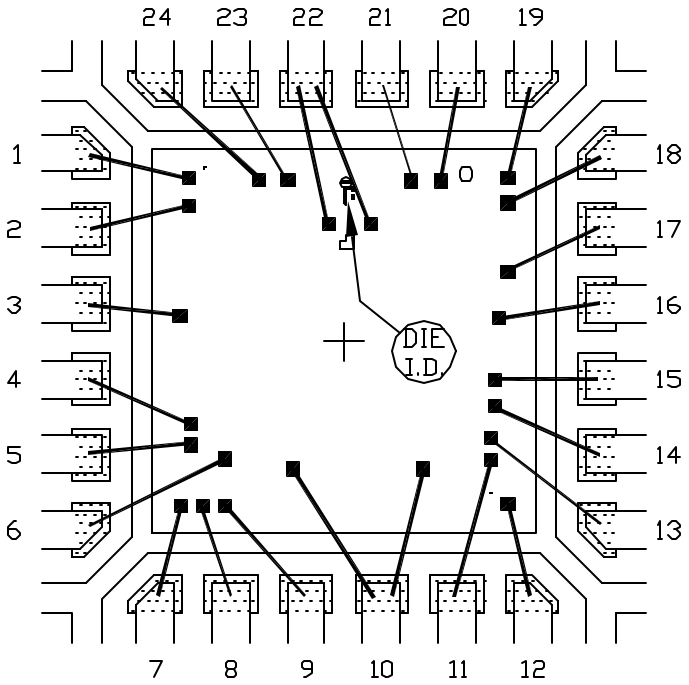
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



4x4x0.8mm THIN QFN PKG. EXPOSED PAD PKG.

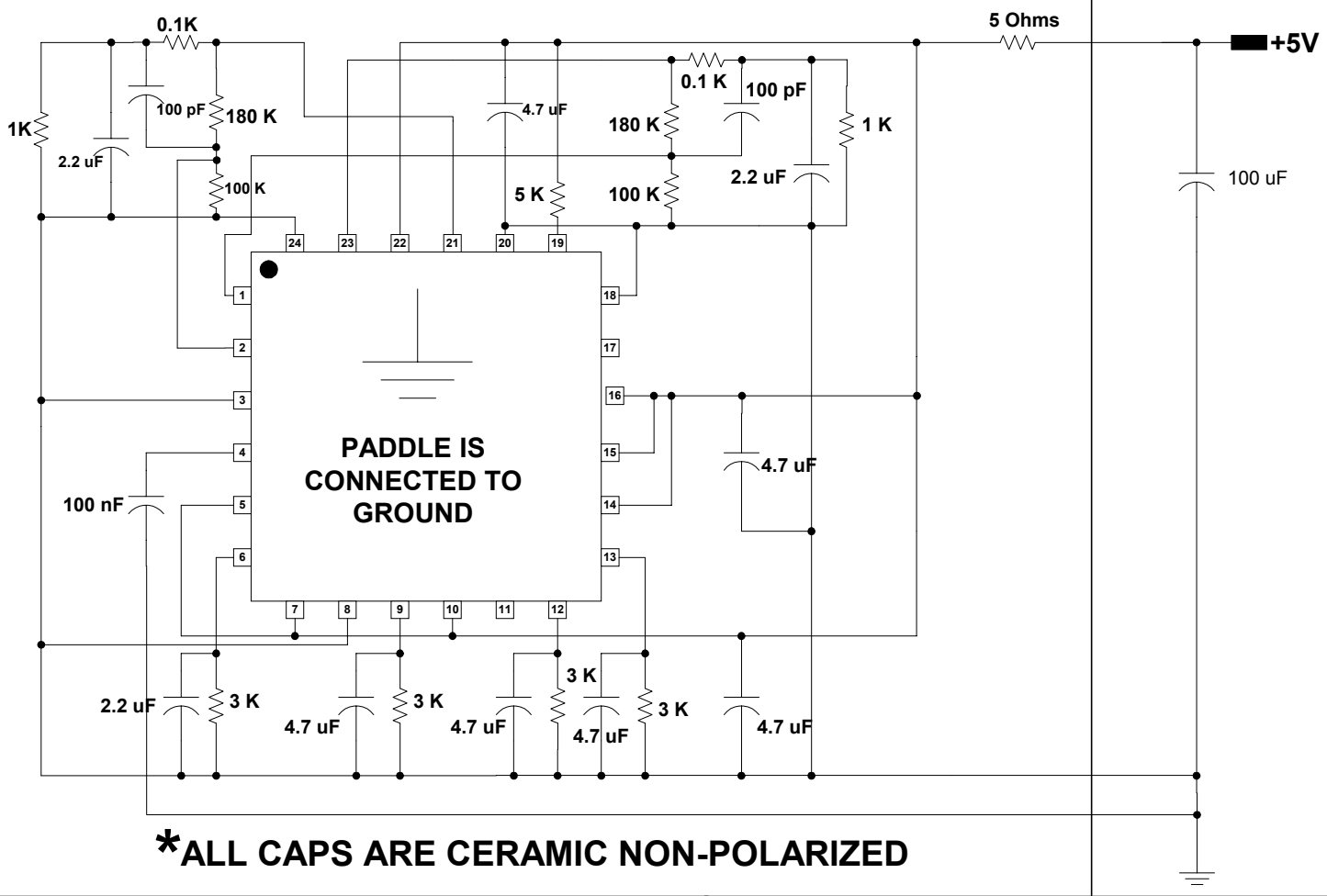


BONDABLE AREA

PKG. CODE: T2444-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 110x110	PKG.			BOND DIAGRAM #: 05-9000-1529	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



***ALL CAPS ARE CERAMIC NON-POLARIZED**

DEVICES: MAX 8621 (PN96)
PACKAGE: 24-QFN (4x4) THIN
MAX. EXPECTED CURRENT = 13mA, TYPICAL = 9mA

NOTES: