

RELIABILITY REPORT
FOR
MAX8620YETD
PLASTIC ENCAPSULATED DEVICES

April 23, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Written by

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Conclusion

The MAX8620Y successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX8620Y micro-power-management integrated circuit (μ PMIC) powers low-voltage microprocessors or DSPs in portable devices. The μ PMIC includes a high efficiency step-down DC-DC converter, two lowdropout linear regulators (LDOs), a microprocessor reset output, and power-on/off control logic. This device maintains high efficiency at light loads with a low 115 μ A supply current, and its miniature TDFN package makes it ideal for portable devices.

The MAX8620Y's step-down DC-DC converter utilizes a proprietary 4MHz hysteretic-PWM control scheme that allows for ultra-small external components. Internal synchronous rectification improves efficiency and eliminates the external Schottky diode that is required in conventional step-down converters. The output voltage is adjustable from 0.6V to 3.3V, with guaranteed output current up to 500mA.

The MAX8620Y's two LDOs offer low 45 μ V_{RMS} output noise and a low dropout of only 200mV at 200mA. Each LDO delivers at least 300mA of continuous output current. The output voltages are pin selectable from 1.8V to 3.3V for flexibility.

A microprocessor reset output (RESET-bar) monitors OUT1 and warns the system of impending power loss allowing safe shutdown. RESET-bar asserts during power-up, power-down, shutdown, and fault conditions where V_{OUT1} is below its regulation voltage.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN1, IN2, PWR_ON, RESET, EN2, SEL1, SEL2, HF_PWR, FB, BP to GND	-0.3V to +6.0V
OUT1, OUT2 to GND	-0.3V to (VIN1 + 0.3V)
LX Current	1.5ARMS
Continuous Power Dissipation (TA = +70°C)	
14-Pin TDFN (derate 18.2mW/°C above +70°C)	1454mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

- A. Description/Function: μ PMIC for Microprocessors or DSPs in Portable Equipment
- B. Process: B8 - Standard 8 micron silicon gate CMOS
- C. Number of Device Transistors: 4481
- D. Fabrication Location: California or Texas, USA
- E. Assembly Location: Thailand
- F. Date of Initial Production: July, 2004

III. Packaging Information

- A. Package Type: **14-Pin QFN (3x3)**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate or 100% Matte Tin
- D. Die Attach: Silver-filled Epoxy
- E. Bondwire: Gold (1.3 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: Buildsheet # 05-9000-1456
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

IV. Die Information

- A. Dimensions: 70 X 94 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: TiW/ AlCu/ TiWN
- D. Backside Metallization: None
- E. Minimum Metal Width: .8 microns (as drawn)
- F. Minimum Metal Spacing: .8 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

△ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 22.91 \times 10^{-9} \quad \lambda = 22.91 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-6422) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**) located on the Maxim website at <http://www.maxim-ic.com>. Current monitor data for the S8/B8 Process results in a FIT Rate of 0.27 @ 25C and 4.64 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PN95 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX8620YETD

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

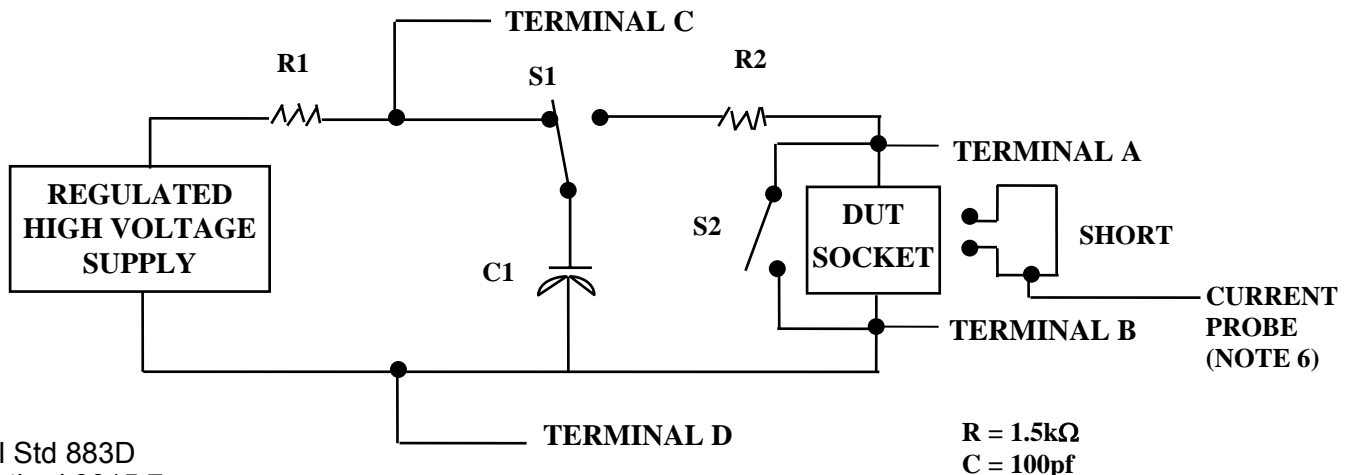
2/ No connects are not to be tested.

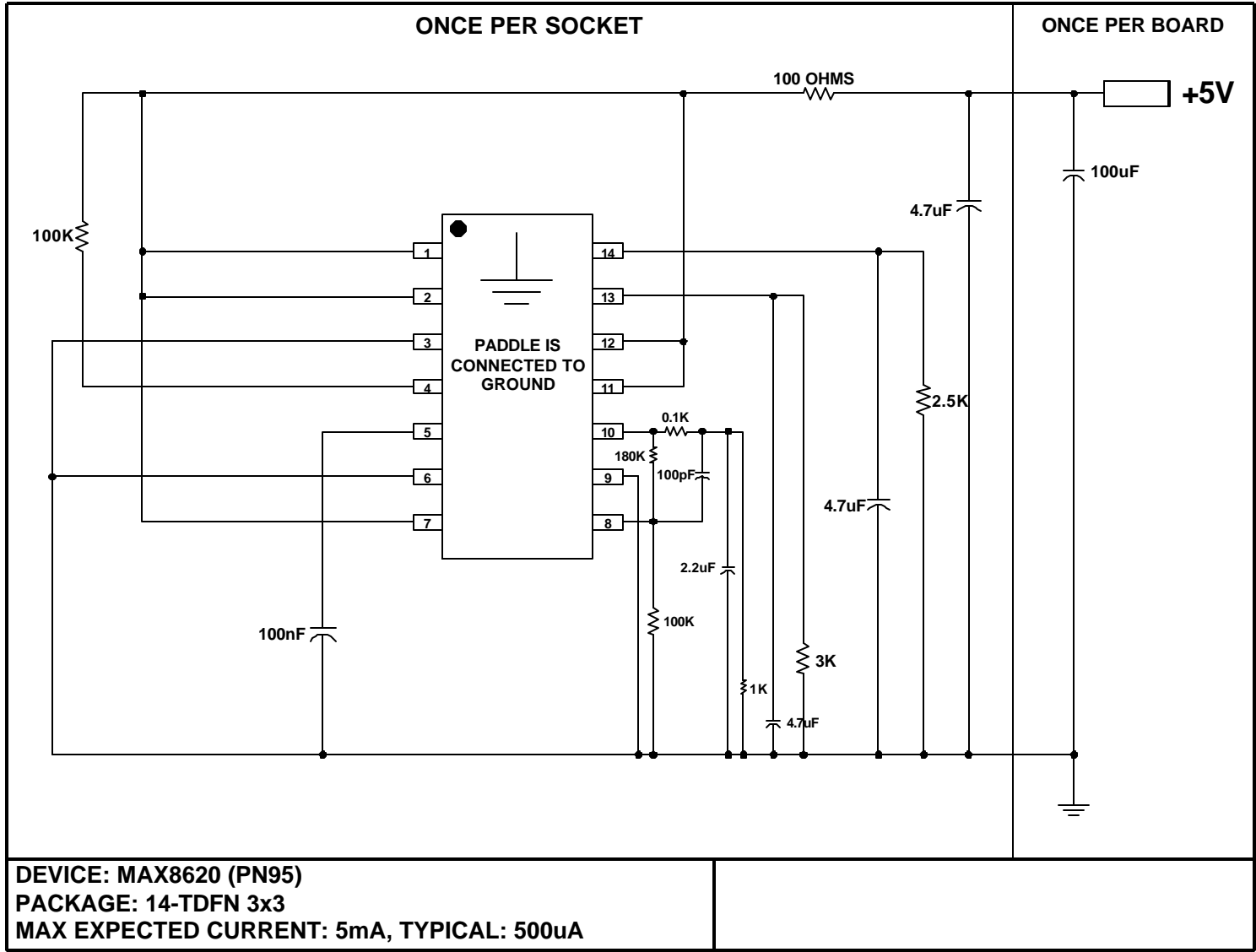
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

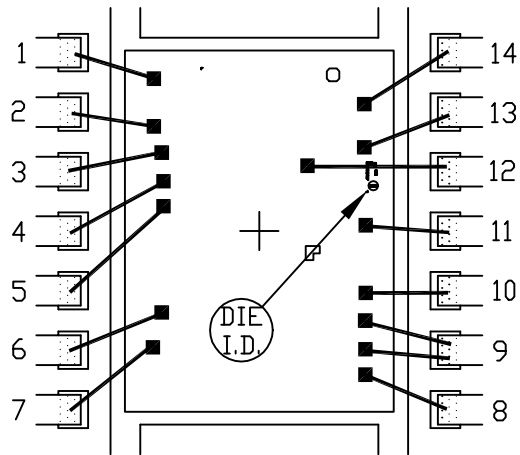
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





3x3x0.80mm TDFN PKG.
0.40mm LEAD PITCH

EXPOSED PAD PKG.



 BONDABLE AREA

PKG. CODE: T1433-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 78x102	PKG. DESIGN			BOND DIAGRAM #: 05-9000-1456	REV: B