

RELIABILITY REPORT  
FOR  
MAX8581ETB+  
(MAX8581/MAX8582)  
PLASTIC ENCAPSULATED DEVICES

December 22, 2008

**MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX8581ETB+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX8581/MAX8582 high-frequency step-down converters are optimized for dynamically powering the power amplifier (PA) in CDMA handsets. They integrate a high-efficiency PWM step-down converter for medium- and low-power transmission and a 60m (typ) bypass mode to power the PA directly from the battery during high-power transmission. They use an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. The MAX8581/MAX8582 use an internal feedback network, and the switching frequency is internally set to 2.5MHz and 1.5MHz, respectively. Fast switching (up to 2.5MHz) and fast soft-start allow the use of ceramic 2.2 $\mu$ F input and output capacitors while maintaining low voltage ripple. The small 1.5 $\mu$ H to 3.3 $\mu$ H inductor size can be optimized for efficiency. The MAX8581/MAX8582 are available in 10-pin, 3mm x3mm TDFN packages (0.8mm max height).

## II. Manufacturing Information

A. Description/Function:	2.5MHz/1.5MHz Step-Down Converters with 60mW Bypass in TDFN for CDMA PA Power
B. Process:	S45
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	ISPL Philippines, UTL Thailand, Unisem Malaysia
F. Date of Initial Production:	October 06, 2006

## III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1173
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.5°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.5°C/W

## IV. Die Information

A. Dimensions:	50 X 62 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)  
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.4 \times 10^{-9}$$

$\lambda = 22.4$  F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the S45ST Process results in a FIT Rate of 0.9 @ 25C and 13.84 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

### C. E.S.D. and Latch-Up Testing

The PN48-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX8581ETB+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
<b>Moisture Testing</b> (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data