

RELIABILITY REPORT  
FOR  
**MAX8530ETTxx**  
PLASTIC ENCAPSULATED DEVICES

May 14, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX8530 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

The MAX8530 offers the benefits of low-dropout voltage and ultra-low power regulation in subminiaturized UCSP and QFN packages with an integrated microprocessor reset circuit. The device operates from a 2.5V to 6.5V input and delivers up to 200mA and 150mA outputs with low dropout of 100mV (typ) at 100mA. Designed with an internal P-channel MOSFET pass transistor, the supply current is kept at a low 130 $\mu$ A (with both LDOs on), independent of the load current and dropout voltage. Other features include short-circuit protection and thermal-shutdown protection.

The MAX8530 provides microprocessor open-drain, active-low reset output to monitor OUT1, eliminating external components and adjustments. The MAX8530 asserts a 100ms (min) RESET-bar signal when OUT1 drops below 87% of the nominal output voltage.

The device includes a logic-controlled shutdown input and is available in 6-bump UCSP and 6-pin thin QFN exposed pad packages.

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN, SHDN, RESET, BP to GND	-0.3V to +7V
OUT1, OUT2 to GND	-0.3V to (VIN + 0.3V)
Output Short-Circuit Duration	Indefinite
Continuous Power Dissipation (TA = +70°C)	
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
6-Lead QFN Lead Temperature (10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
6-Lead QFN	1951mW
Derates above +70°C	
6-Lead QFN	24.4mW/°C

## II. Manufacturing Information

A. Description/Function:	Dual Low-Dropout Linear Regulators with RESETor Low-Noise Output
B. Process:	S8
C. Number of Device Transistors:	1720
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	January, 2003

## III. Packaging Information

A. Package Type:	<b>6-Lead QFN(3x)</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0297
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

## IV. Die Information

A. Dimensions:	64 x 48 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

### A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 22.62 \times 10^{-9} \quad \lambda = 22.62 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6099) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The PN04 die type has been found to have all pins able to withstand a transient pulse of 1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX8530ETTxx**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test</b> (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
<b>Moisture Testing</b> (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data

## Attachment #1

TABLE II. Pin combination to be tested. <sup>1/</sup> <sub>2/</sub>

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <sup>3/</sup>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

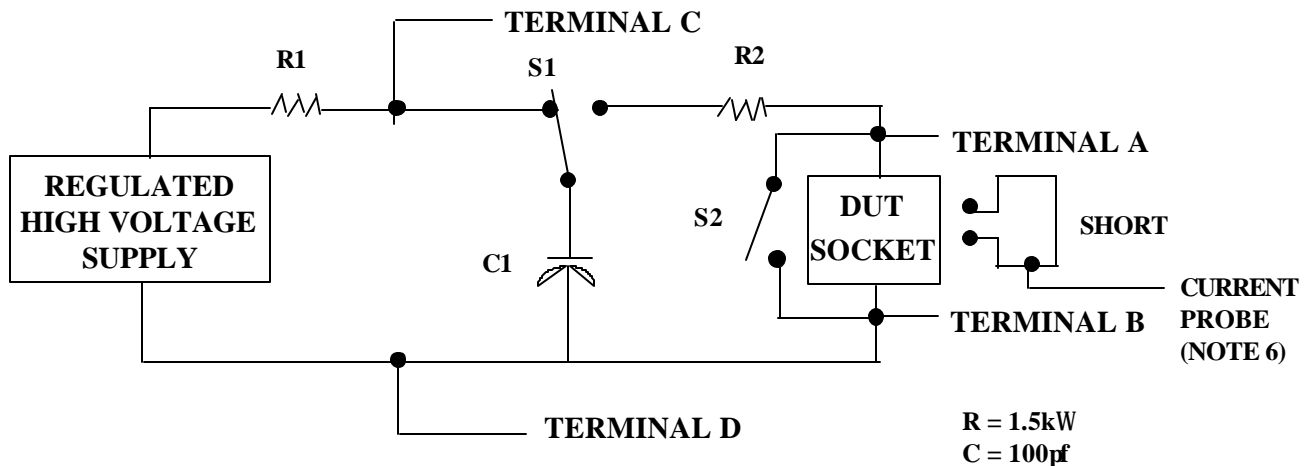
<sup>1/</sup> Table II is restated in narrative form in 3.4 below.

<sub>2/</sub> No connects are not to be tested.

<sup>3/</sup> Repeat pin combination I for each named Power supply and for ground (e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

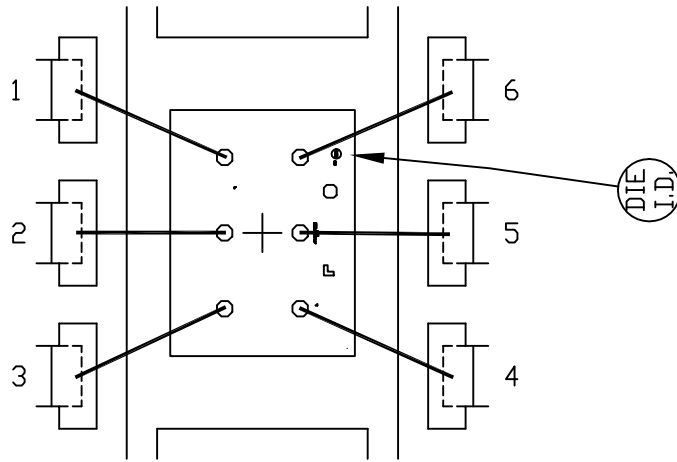
### 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



3x3x0.8 MM QFN THIN PKG.

EXPOSED PAD PKG.



PKG. CODE: T633-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 71x102	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0297	REV: A

