MAX8525EEI
Rev. A

RELIABILITY REPORT

FOR

MAX8525EEI

PLASTIC ENCAPSULATED DEVICES

August 9, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX8525 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation
IV. .....Die Information
.....Attachments

I. Device Description

A. General

The MAX8525 (VRM 10/VRD 10) current-mode step-down controller provides flexible, low-cost, low-voltage CPU core supplies

The switching frequency of the MAX8525 is adjustable from 150kHz to 1.2MHz, permitting loop bandwidths of up to 200kHz. Peak current-mode control provides fast transient response and reduces cost. A proprietary current-sharing scheme reduces current imbalance between phases to less than 5% at full load.

The MAX8525 offers 0.4% initial accuracy and remote-sense functionality. The controller also feature programmable no-load offset and output-voltage positioning to adjust the output voltage as a function of the output current. The fast-active voltage positioning further reduces bulk output capacitors and cost.

Current-mode control also simplifies compensation with a variety of capacitors by eliminating the output-filter double pole associated with voltage-mode controllers. The device is compatible with electrolytic, tantalum, polymer, and ceramic capacitors. Output current sensing eliminates issues associated with controllers that use high-side current sense and ensure stable and jitter-free operation. Temperature-compensated, lossless inductor current sense eliminates the need for a current-sense resistor and further reduces cost, while maintaining voltage-positioning accuracy and reducing power dissipation.

The MAX8525 features control VID voltage transition for dynamic VID changes and eliminate both undervoltage and overvoltage overshoot. The PWRGD signal is accurate during VID code changes for the MAX8525 to avoid any false fault signal. Adjustable foldback current-limit and overvoltage protection provide for a robust design.

B. Absolute Maximum Ratings

Item	Rating
REF, COMP, VID0 to VID5, OSC, CLKI, CLKO to GND	-0.3V to VCC + 0.3V
RS+, RS-, ILIM to GND	-0.3V to VCC + 0.3V
PWM_ to GND	-0.3V to VCC + 0.3V
EN, PWRGD, VCC to GND	-0.3V to +6V
CS1_3-, CS2_4-, CS_+ to GND	-0.3V to VCC + 0.3V
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin QSOP	860mW
Derates above +70°C	
28-Pin QSOP	10.8mW/°C

II. Manufacturing Information

A. Description/Function: 2- to 8-Phase VRM 10/9.1 PWM Controllers with Precise Current Sharing and Fast Voltage Positioning

B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	9021
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	May, 2003

III. Packaging Information

A. Package Type:	**28-Pin QSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0380
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	86 x 132 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$

$\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6116) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PM51-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8525EEI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

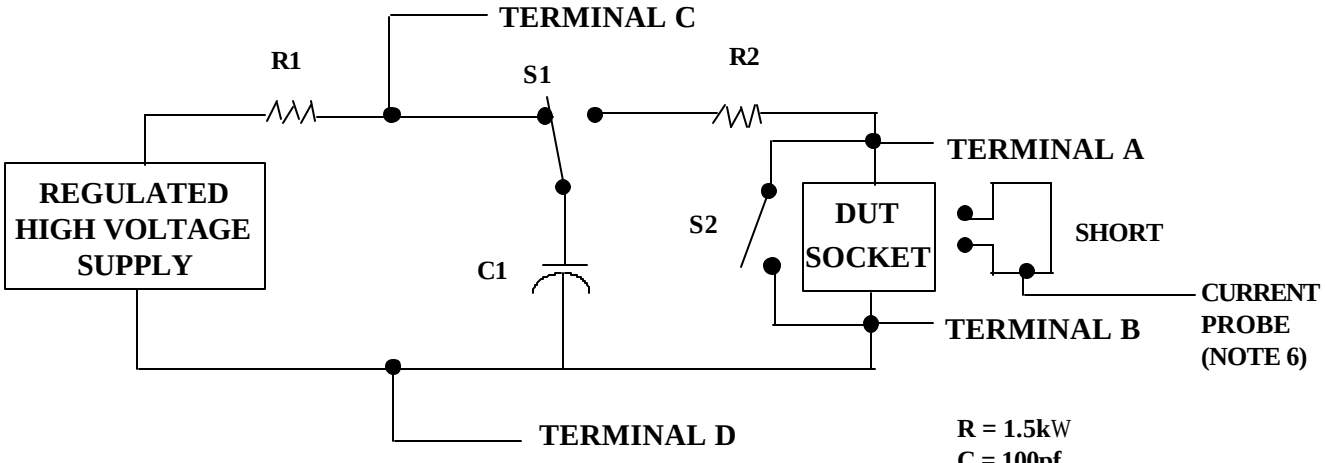
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

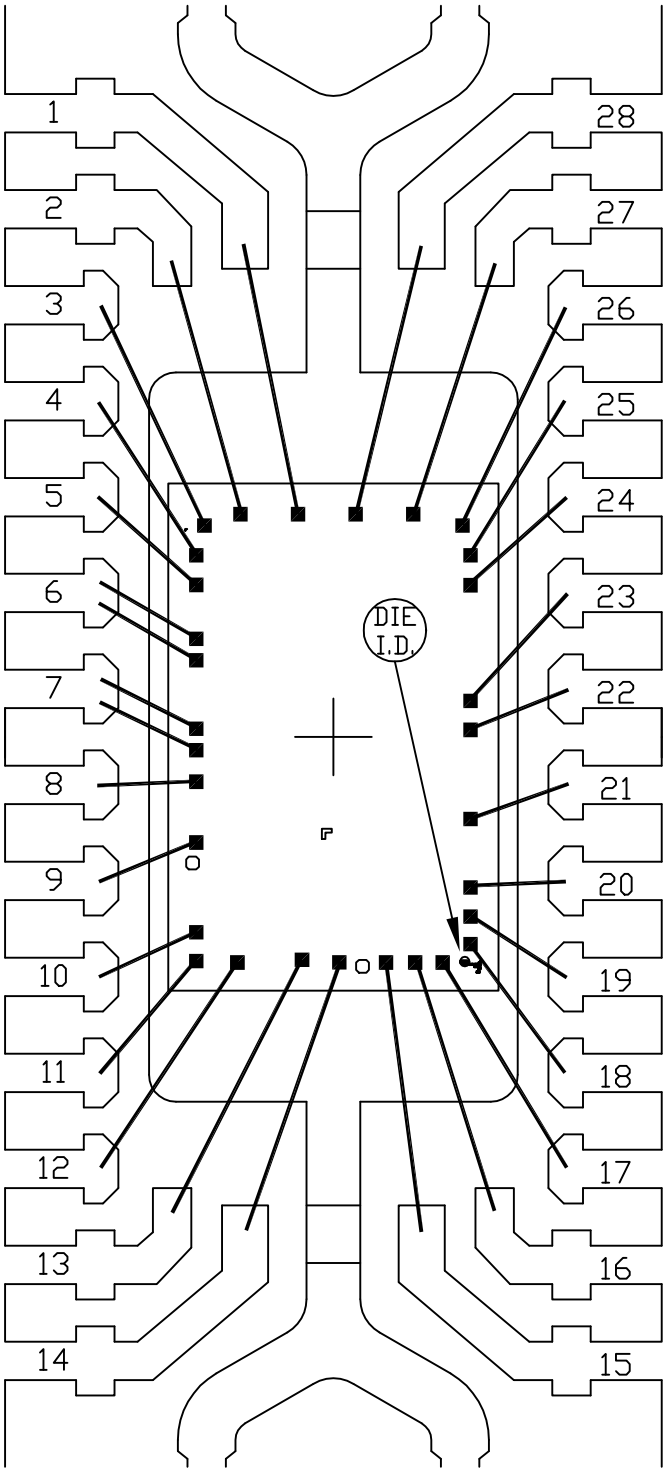
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

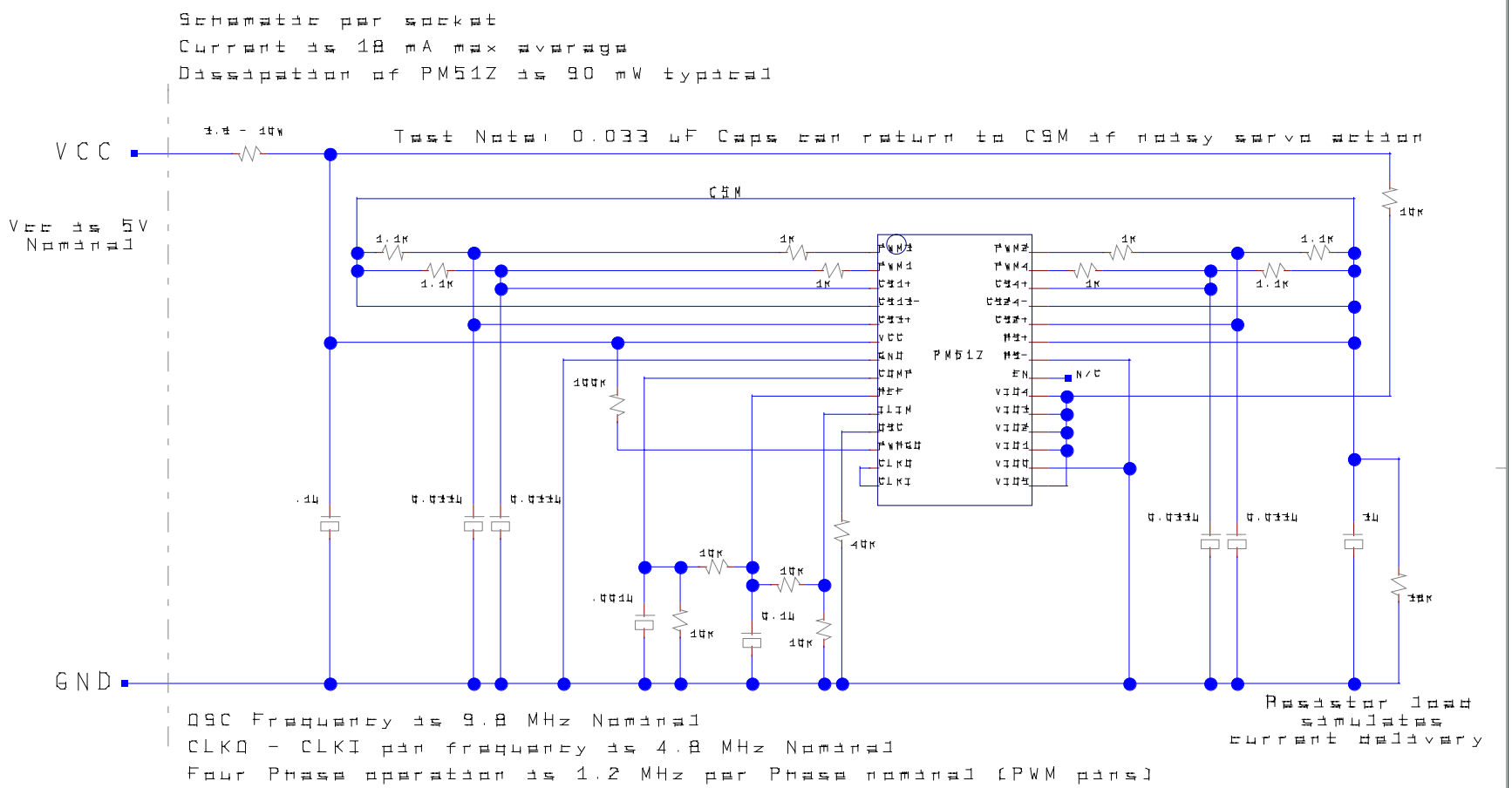
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: E28-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X190	PKG.			BOND DIAGRAM #: 05-9000-0380	REV: A
	DESIGN				



MAXIM	TITLE: BI Circuit (MAX8524/8525) PM51		
	DOCUMENT I.D. 06-6116	REVISION A	PAGE 2