RELIABILITY REPORT FOR

MAX77734

WAFER LEVEL DEVICES

September 24, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX77734 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX77734 is a tiny PMIC for applications where size and simplicity are critical. The IC integrates a linear-mode Li+ battery charger, low-dropout linear regulator (LDO), analog multiplexer, and dual-channel current sink driver. The charger is designed for small-battery systems that require accurate termination as low as 0.375mA. The circuit can instantly regulate the system voltage when an input source is connected even if the battery is depleted. The 150mA LDO's output is programmable between 0.8V and 3.975V with I2C. The analog MUX enables an external ADC to perform conversions on battery V&I signals for power monitoring. The current sinks are capable of sinking 12.8mA each and can be programmed for LEDs to blink in custom patterns. The MAX77734 is available in a 20-bump wafer-level package (WLP). For a similar product with additional regulators, see the MAX77650.

II. Manufacturing Information

A. Description/Function:	Ultra-Low Power Tiny PMIC with Power Path Charger for Small Li+ and 150mA LDO
B. Process:	S18
C. Number of Device Transistors:	93186
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	July 5, 2017

III. Packaging Information

A. Package Type:	20-bump WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Bondwire:	N/A (N/A mil dia.)
E. Assembly Diagram:	#05-100630
F. Flammability Rating:	Class UL94-V0
G. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
H. Single Layer Theta Ja:	N/A°C/W
I. Single Layer Theta Jc:	N/A°C/W
J. Multi Layer Theta Ja:	55.49°C/W
K. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	88.9764X78.7401 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The MD34-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX77734

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.