RELIABILITY REPORT

FOR

MAX77231EZL+T

WAFER LEVEL DEVICES

October 18, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

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Conclusion

The MAX77231EZL+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX77231 is optimized for boost applications, requiring very low ripple/noise and small PCB space. Output ripple and noise are suppressed to 35µVRMS (in 1MHz BW) by a PMOS linear post-regulator set 0.5V below the boost regulator output to reject noise while optimizing efficiency.

The boost regulator operates using a 1µH/400mA inductor and 2.2µF (0.22 (min) after derating) output capacitance. Fast transient response and stable operation are guaranteed using a current-limited PFM architecture.

A PMOS low-noise linear post-regulator attenuates boost converter ripple by ～50dB (10MHz BW) before delivering 11.2V to the load. Other output voltages up to 16.2V can be factory set. The LDO also disconnects the load from the boost during shutdown, allowing the output to fall to 0V (true shutdown). Active discharge can also be activated.

The MAX77231 is packaged in a 9-bump wafer-level package (WLP), providing a compact layout when combined with the inductor and external capacitors. Total solution size is less than 7mm2.

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II. Manufacturing Information

A. Description/Function: 2.75V to 4.8V Input, 10mA Output, 35µV_{RMS} Ultra Low Noise and Ripple Boost Regulator

B. Process: S18

C. Number of Device Transistors: 11998

D. Fabrication Location: USA

E. Assembly Location: USA

F. Date of Initial Production: December 09, 2014

III. Packaging Information

A. Package Type: 9-bump Thin WLP

B. Lead Frame: N/A

C. Lead Finish: N/A

D. Die Attach: None

E. Bondwire: N/A (N/A mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: #05-9000-5251

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 1

J. Single Layer Theta Ja: N/A°C/W

K. Single Layer Theta Jc: N/A°C/W

L. Multi Layer Theta Ja: 83°C/W

M. Multi Layer Theta Jc: N/A°C/W

IV. Die Information

A. Dimensions: 50X50 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: 0.23 microns (as drawn)

F. Minimum Metal Spacing: 0.23 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PB18-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX77231EZL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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