RELIABILITY REPORT

FOR

MAX755ESA+

PLASTIC ENCAPSULATED DEVICES

February 18, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
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Conclusion

The MAX755ESA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX735 and MAX755 are CMOS, inverting switchmode regulators with intemal power MOSFETs. The MAX755 operates from a +2. 7V to +9V input and generates an adjustable negative output; 1 W output power is guaranteed when powered from a +4.5V input. The MAX735 operates from a +4.0V to +6.2V output; 200mA output current is guaranteed for inputs greater than +4.5V. Quiescent supply current for the MAX735 is typically 1.6mA, and a shutdown mode reduces this to 10flA. These powerconserving features, along with high efficiency and applications circuits that lend themselves to miniaturization, make the MAX735/MAX755 excel in a broad range of on-card and portable-equipmenl applications.

The MAX735/MAX755 employ a high-performance currentmode pulse-width modulation (PWM) control scheme to provide tight output-voltage regulation and low subharmonic noise. The fixed-frequency oscillator is factorytrimmed to 160kHz, allowing for easy noise filtering. The regulators are production tested in actual application circuits, and output accuracy is guaranteed to within ±5% over all specified conditions of line, load, and temperature. The input-to-output differential of the MAX755 is limited to VIN + IVOUTI is less than or equal to 11.7V.

For an adjustable-output device with a wider input voltage range, refer to the MAX759 data sheet. For a fixed -5V part with a wider input voltage range, refer to the MAX739 data sheet. For fixed -12V and -15V versions, see the MAX736 and MAX737 data sheets. For lower-power applications, refer to the MAX635/636/637 data sheet.

II. Manufacturing Information

A. Description/Function:	-5V, Inverting, PWM DC-DC Converter
B. Process:	S3
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines, Thailand, Malaysia
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	8-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0701-0729
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	170°C/W
K. Single Layer Theta Jc:	40°C/W
L. Multi Layer Theta Ja:	132°C/W
M. Multi Layer Theta Jc:	38°C/W

IV. Die Information

A. Dimensions:	72X116 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 370 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 2.97 \times 10^{-9}$

$\lambda = 2.97$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S3 Process results in a FIT Rate of 0.03 @ 25C and 0.5 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot NYQFHB027A, D/C 0749)

The PS43-5 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-150mA.

Table 1

Reliability Evaluation Test Results

MAX755ESA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	NQGADU004A, D/C 9822
	Biased	& functionality	50	0	XYQAXB060B, D/C 9703
	Time = 192 hrs.		80	0	XYQFGB059A, D/C 9707
			80	0	XYQEHB058A, D/C 9707
			80	0	XYQCXA061A, D/C 9703

Note 1: Life Test Data may represent plastic DIP qualification lots.