

RELIABILITY REPORT
FOR
MAX7462USA+T
PLASTIC ENCAPSULATED DEVICES

October 8, 2012

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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| Approved by |
| Sokhom Chum |
| Quality Assurance |
| Reliability Engineer |

Conclusion

The MAX7462USA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

| | |
|-----------------------------------|--------------------------------------|
| I.Device Description | IV.Die Information |
| II.Manufacturing Information | V.Quality Assurance Information |
| III.Packaging Information | VI.Reliability Evaluation |
|Attachments | |

I. Device Description

A. General

The MAX7462/MAX7463 single-channel, standard-definition, integrated video reconstruction filters and buffers are ideal for anti-aliasing and digital-to-analog smoothing video applications or wherever analog video is reconstructed from digital data (such as cable/satellite/terrestrial set-top boxes and DVRs). The MAX7462 includes a disable function, which places the output in a high-impedance state allowing multiplexing of multiple output signals. It also has an external gain control that sets the output buffer gain to either +6dB or +9.5dB. The higher gain setting allows a lower DAC output signal than the standard 1VP-P signal. The MAX7463 output buffer has a fixed gain of +6dB. The MAX7462/MAX7463 operate from a single +5V supply and have a flat passband out to 5MHz with a stopband attenuation of -43dB (typ) at 27MHz. These devices can drive two standard 150 AC-coupled or DC-coupled video loads. The output black level of the MAX7462/MAX7463 is less than 1V for DC-coupled outputs. The MAX7462 is available in an 8-pin μ MAX® package and an 8-pin SO package. The MAX7463 is available in an 8-pin SO package. All devices are specified over the 0°C to +85°C temperature range.

II. Manufacturing Information

| | |
|----------------------------------|---|
| A. Description/Function: | Single-Channel Video Reconstruction Filters and Buffers |
| B. Process: | C6 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | California |
| E. Assembly Location: | Malaysia, Thailand, Philippines |
| F. Date of Initial Production: | October 22, 2005 |

III. Packaging Information

| | |
|--|--------------------------|
| A. Package Type: | 8-pin SOIC (N) |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-1901 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 170°C/W |
| K. Single Layer Theta Jc: | 40°C/W |
| L. Multi Layer Theta Ja: | 136°C/W |
| M. Multi Layer Theta Jc: | 38°C/W |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 55 X 56 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SI1AAQ001E, D/C 0527)

The VP20 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX7462USA+

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|----------------------------------|---|----------------------------------|-------------|--------------------|----------------------|
| Static Life Test (Note 1) | Ta = 135°C Biased Time = 192 hrs. | DC Parameters & functionality | 48 | 0 | S11AAQ001C, D/C 0527 |

Note 1: Life Test Data may represent plastic DIP qualification lots.