

RELIABILITY REPORT  
FOR  
MAX7404ESA+  
PLASTIC ENCAPSULATED DEVICES

December 3, 2013

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

<b>Approved by</b>
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## Conclusion

The MAX7404ESA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX7400/MAX7403/MAX7404/MAX7407 8th-order, lowpass, elliptic, switched-capacitor filters (SCFs) operate from a single +5V (MAX7400/MAX7403) or +3V (MAX7404/MAX7407) supply. These devices draw 2mA of supply current and allow corner frequencies from 1Hz to 10kHz, making them ideal for low-power anti-aliasing and post-DAC filtering applications. They feature a shutdown mode that reduces the supply current to 0.2 $\mu$ A. Two clocking options are available: self-clocking (through the use of an external capacitor) or external clocking for tighter cutoff-frequency control. In addition, an offset adjustment pin (OS) allows for the adjustment of the DC output level. The MAX7400/MAX7404 provide 82dB of stopband rejection and a sharp rolloff with a transition ratio of 1.5. The MAX7403/MAX7407 provide a sharper rolloff with a transition ratio of 1.2, while still delivering 60dB of stopband rejection. The fixed response of these devices simplifies the design task to corner-frequency selection by setting a clock frequency. The MAX7400/MAX7403/MAX7404/MAX7407 are available in 8-pin SO and DIP packages.

## II. Manufacturing Information

A. Description/Function:	8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters
B. Process:	B12
C. Number of Device Transistors:	1120
D. Fabrication Location:	Oregon, California or Texas
E. Assembly Location:	Philippines, Thailand, or Malaysia
F. Date of Initial Production:	June 11, 1999

## III. Packaging Information

A. Package Type:	8-pin SOIC (N)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0201-0123
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	170 °C/W
K. Single Layer Theta Jc:	40 °C/W
L. Multi Layer Theta Ja:	128.4 °C/W
M. Multi Layer Theta Jc:	36 °C/W

## IV. Die Information

A. Dimensions:	85X126 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the B12 Process results in a FIT Rate of 0.05 @ 25C and 0.92 @ 55C (0.8 eV, 60% UCL).

### B. E.S.D. and Latch-Up Testing (ESD lot IR7ECA006C D/C 0019, Latch-Up lot NR7EDA014A D/C 0524)

The AF15-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX7404ESA+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	IR7KBQ001A, D/C 9908

Note 1: Life Test Data may represent plastic DIP qualification lots.