

RELIABILITY REPORT
FOR
MAX7042ATJ+
PLASTIC ENCAPSULATED DEVICES

November 11, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
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Approved by
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Quality Assurance
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Conclusion

The MAX7042ATJ+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX7042 fully integrated, low-power, CMOS superheterodyne RF receiver is designed to receive frequency-shift-keyed (FSK) data at rates up to 66kbps nonreturn-to-zero (NRZ) (33kbps Manchester). The MAX7042 requires only a few external components to realize a complete wireless RF receiver at 308, 315, 418, and 433.92MHz. The MAX7042 includes all the active components required in a superheterodyne receiver including a low-noise amplifier (LNA), an image-rejection (IR) mixer, a fully integrated phase-locked loop (PLL), local oscillator (LO), 10.7MHz IF limiting amplifier with received-signal-strength indicator (RSSI), low-noise FM demodulator, and a 3V regulator. Differential peak-detecting data demodulators are included for baseband data recovery. The MAX7042 is available in a 32-pin thin QFN and is specified over the automotive -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	308MHz/315MHz/418MHz/433.92MHz Low-Power, FSK Superheterodyne Receiver
B. Process:	0.35UM 2 Poly 3 Metal CMOS
C. Number of Device Transistors:	7946
D. Fabrication Location:	Taiwan
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	April 23, 2005

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1611
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	1.7°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	90 X 72 mils
B. Passivation:	Silicon Dioxide/Silicon Nitride
C. Interconnect:	Al/Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35um
F. Minimum Metal Spacing:	0.35um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	Silicon Dioxide
I. Die Separation Method:	Wafer Saw:

V. Quality Assurance Information

- | | |
|-----------------------------------|-------------------------------------------------------------------------------------------------|
| A. Quality Assurance Contacts: | Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation
A. Accelerated Life Test

The results of the biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.4 \times 10^{-9}$$

$$\lambda = 22.4 \text{ F.I.T. (60\% confidence level @ 25}^\circ\text{C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the TS352P3M Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The LF12 die type has been found to have all pins able to withstand a transient pulse of +/-2000 V HBM; +/-150 V MM per JEDEC JESD22-A114/5. Latch-Up testing has shown that this device withstands a current of 250 mA.

Table 1
Reliability Evaluation Test Results

MAX7042ATJ+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data