

RELIABILITY REPORT
FOR
MAX701xxA
PLASTIC ENCAPSULATED DEVICES

June 16, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX701 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	
IV.Die InformationAttachments

I. Device Description

A. General

The MAX701 is a supervisory circuit used to monitor the power supplies in μ P and digital systems. The /RESET/RESET outputs of the MAX701 are guaranteed to be in the correct state for V_{CC} voltages down to +1V. This device provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V powered circuits.

The MAX701 has both /RESET and RESET outputs. Their primary function is to provide a system reset. Accordingly, an active reset signal is supplied for low supply voltages and for at least 200ms after the supply voltage reaches its operating value.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V_{CC}	-0.3V to +15.5V
Voltage (with respect to GND) at RESET, /RESET, HYST, CTL, SENSE	-0.3V to V_{CC}
Rate of Rise, V_{CC}	100V/ μ s
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	471mW
Derates above +70°C	5.9mW/°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin PDIP	727mW
8-Pin NSO	471mW
Derates above +70°C	
8-Pin PDIP	9.1mW/°C
8-Pin NSO	5.9mW/°C

II. Manufacturing Information

A. Description/Function:	Power-Supply Monitor with Reset
B. Process:	SMG (M6-Standard 6 micron metal gate CMOS)
C. Number of Device Transistors:	488
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	January, 1992

III. Packaging Information

A. Package Type:	8-Lead NSO	8-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0701-0319	# 05-0701-0318
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	76 x 120 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	6 microns (as drawn)
F. Minimum Metal Spacing:	6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: : Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 2920 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 0.82 \times 10^{-9}$$

$$\lambda = 0.82 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-0526) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PS53-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 100\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX701xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		2920	1
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	DIP NSO	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

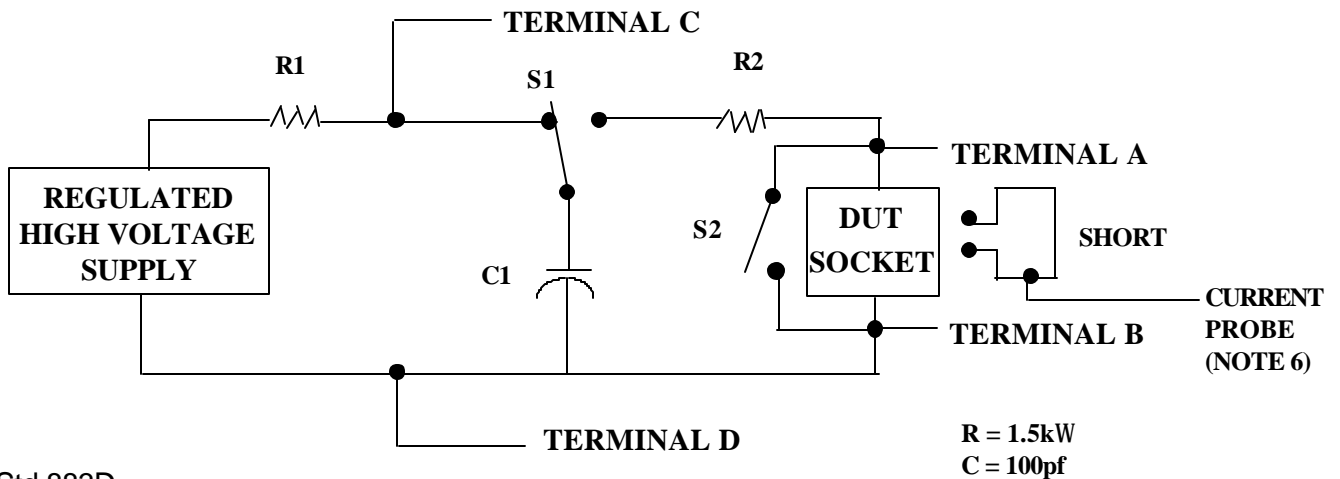
2/ No connects are not to be tested.

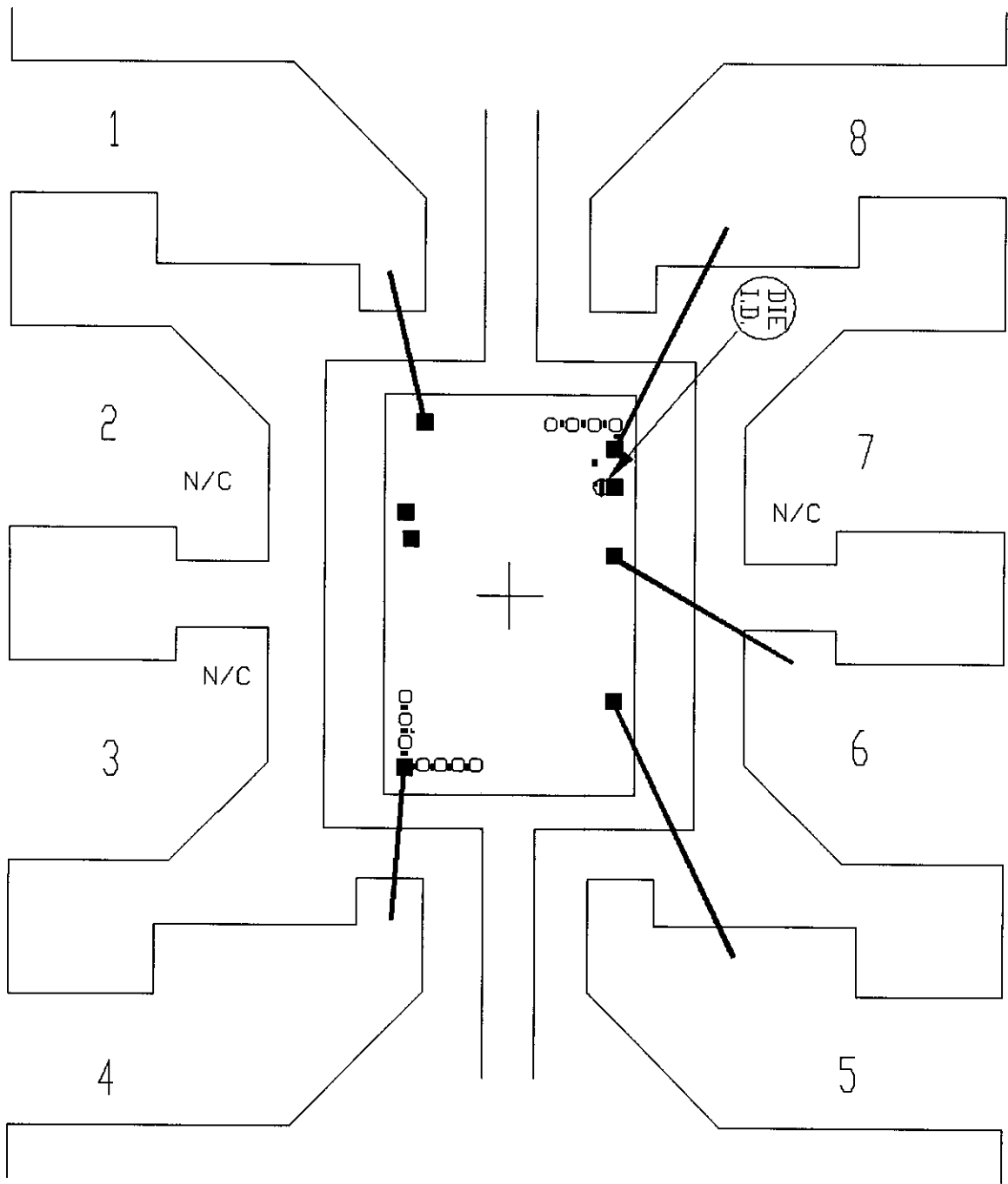
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

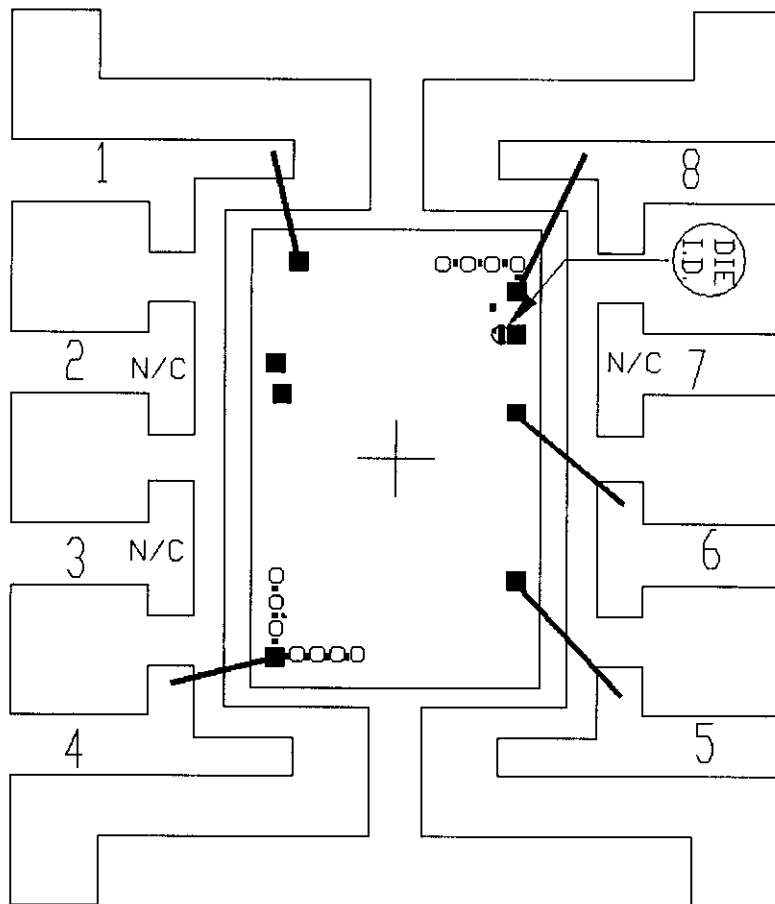
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

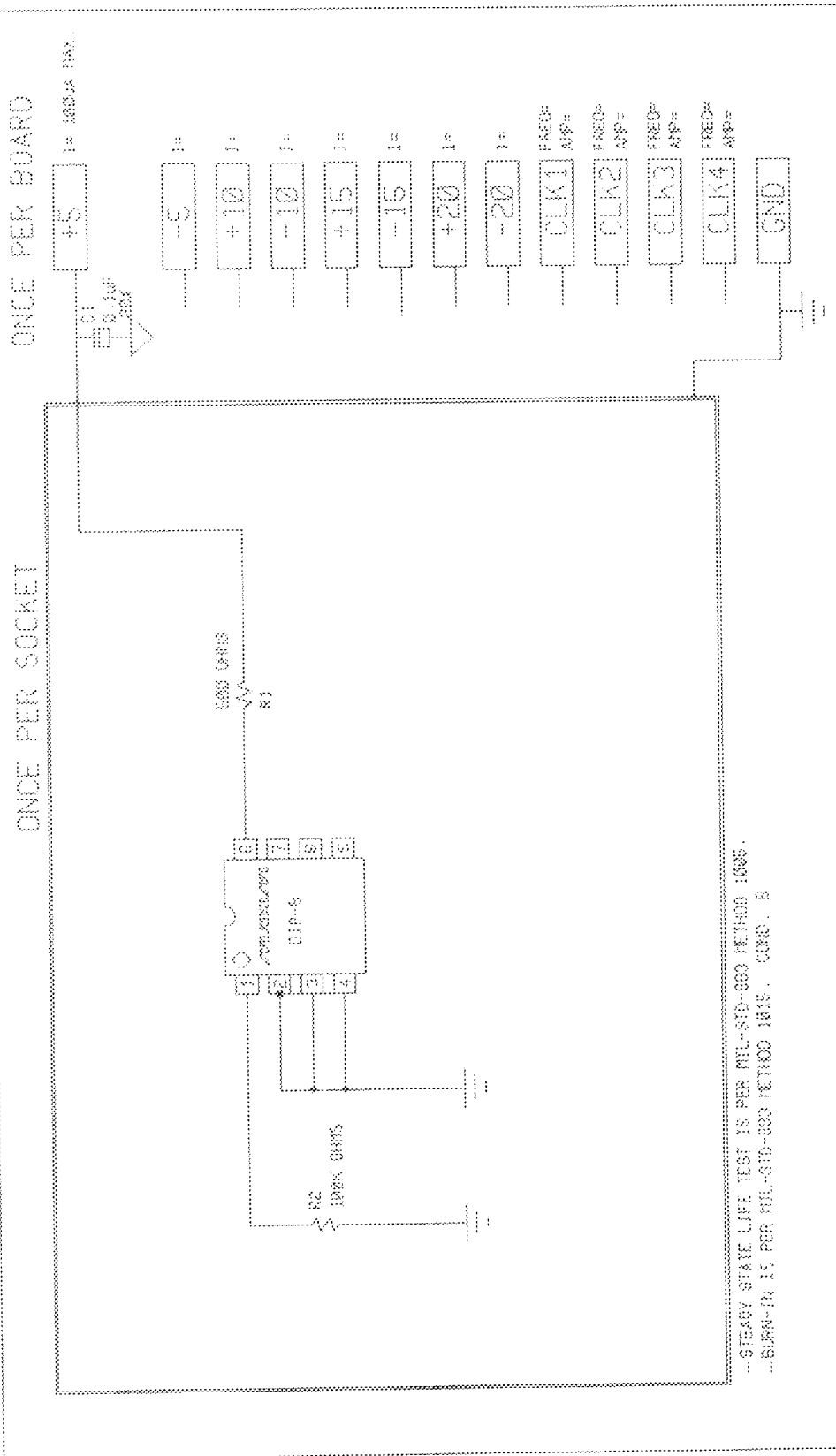




PKG. CODE: P8-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 110 X 140	PKG. DESIGN		OCT 29 1996	BUILDSHEET NUMBER: 05-0701-0319	REV.: C
			11/12/96		



PKG.CODE: S8-4		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 90 X 130	PKG.	[REDACTED]	29 1996	BUILDSHEET NUMBER:	REV.:
	DESIGN		11/12/96.	05-0701-0318	C



ONCE PER SOCKET

ONCE PER BOARD

-- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
 -- BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

<p>NOTES:</p> <ol style="list-style-type: none"> TEMPERATURE: 125C OR EQUIVALENT TIME: 168 HOURS MIN. OR EQUIVALENT ALL COMPONENTS AND MATERIAL MUST STAND 155C ENVIRONMENT APPROVED FOR EX: COMMERCIAL (X) MR/883 	<p>SPEC. NO. 06-526 REV. E</p>	<p>MAXIM BURN-IN SCHEMATIC</p>
<p>DATE: 11/24/95</p>	<p>DEVELOPER: MAX980/698A/692/693A/694 MAX200/781/783/784/790 MAX984/885/895 MAX 917/818/819</p>	
<p>DRAWN BY: C. JONES</p>		