

RELIABILITY REPORT
FOR
MAX6854UK19D1+
PLASTIC ENCAPSULATED DEVICES

February 8, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX6854UK19D1+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX6854/MAX6855/MAX6856/MAX6858/MAX6860-MAX6869 ultra-low-current (170nA, typ) microprocessor (μ P) supervisory circuits combine voltage monitoring, watchdog timer, and manual reset input functions in a 5-pin SOT23 package. These devices assert a reset signal whenever the monitored voltage drops below the factory-trimmed reset threshold voltage, manual reset is asserted, or the watchdog timer expires. The reset output remains asserted for a minimum timeout period after VCC rises above the reset threshold and manual reset is deasserted. Factory-trimmed reset threshold voltages are offered from +1.575V to +4.625V in approximately 100mV increments (see the *Threshold Suffix Guide* in the full data sheet). Each device is offered with six minimum reset timeout options, ranging from 10ms to 1200ms. The MAX6854/MAX6855/MAX6856/MAX6858/MAX6860-MAX6869 are offered in a variety of configurations (see the *Selector Guide* in the full data sheet). The MAX6854/MAX6855/MAX6856/MAX6861-MAX6869 provide a manual reset input, MR-bar. The MAX6864-MAX6869 offer a watchdog timer that monitors activity at the WDI input to prevent code execution errors. The MAX6864-MAX6869 offer watchdog timeout options of 3.3s or 209s (typ). The MAX6861/MAX6862/MAX6863 feature a pin-selectable reset delay period of 10ms or 150ms (min). Push-pull active-low, push-pull active-high, and open-drain active-low reset outputs are available.

II. Manufacturing Information

A. Description/Function:	Nanopower μ P Supervisory Circuits with Manual Reset and Watchdog Timer
B. Process:	C6
C. Number of Device Transistors:	413
D. Fabrication Location:	California
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	July 23, 2004

III. Packaging Information

A. Package Type:	5-pin SOT23
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0553
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	324.3°C/W
K. Single Layer Theta Jc:	82°C/W
L. Multi Layer Theta Ja:	255.9°C/W
M. Multi Layer Theta Jc:	81°C/W

IV. Die Information

A. Dimensions:	42 X 55 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 79 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 2.7 \times 10^{-9}$$

$$\lambda = 2.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot IQ0000034B D/C 0418)

The MS79 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX6854UK19D1+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	79	0	SFJ0DQ002D, D/C 0622

Note 1: Life Test Data may represent plastic DIP qualification lots.