

RELIABILITY REPORT  
FOR  
**MAX6823xUK**  
PLASTIC ENCAPSULATED DEVICES

January 22, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX6823 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX6823 is a low-voltage microprocessor ( $\mu$ P) supervisory circuit that combines voltage monitoring, watchdog timer, and manual reset input functions in a 5-pin SOT23 package. Microprocessor supervisory circuits significantly improve system reliability and accuracy compared to separate ICs or discrete components. This device asserts a reset signal whenever the monitored voltage drops below its preset threshold, keeping it asserted for a minimum timeout period after  $V_{CC}$  rises above the threshold. In addition, a watchdog timer monitors against code execution errors. A debounced manual reset is also available. The MAX6822 monitor voltages from +1.8V to +5.0V. This output is guaranteed to be in the correct state for  $V_{CC}$  down to +1.0V.

Nine preprogrammed reset threshold voltages are available (see *Threshold Suffix Guide*). The MAX6823 has a manual reset input and a watchdog timer and an push-pull RESET-bar.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VCC to GND	-0.3V to +6.0V
Push-Pull RESET, RESET, MR, WDI	-0.3V to (VCC + 0.3V)
Input Current (VCC)	20mA
Output Current (RESET, RESET)	20mA
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
5-Pin SOT23	571mW
Derates above +70°C	
5-Pin SOT23	7.1mW/°C

## II. Manufacturing Information

A. Description/Function:	Low-Voltage SOT23 $\mu$ P Supervisors with Manual Reset and Watchdog Timer
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	750
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	December, 2001

## III. Packaging Information

A. Package Type:	<b>5-Pin SOT23</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0124
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

## IV. Die Information

A. Dimensions:	45 x 35 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	$\text{SiO}_2$
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)  
Bryan Preeshl (Executive Director)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 316 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 3.44 \times 10^{-9}$$

$$\lambda = 3.44 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5652) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The MS61 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX6823xUK**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		316	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

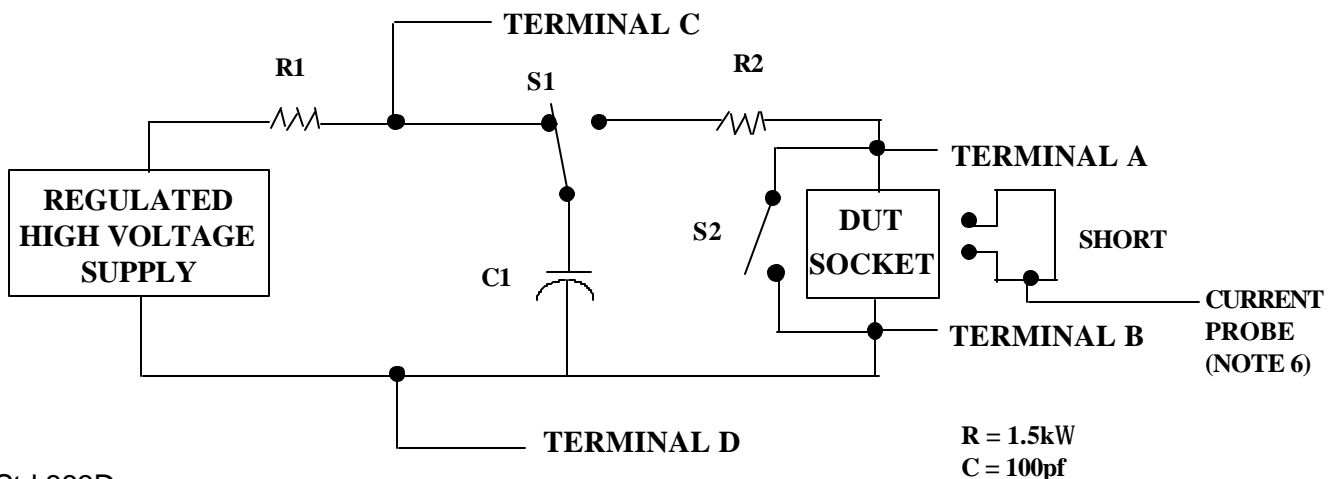
2/ No connects are not to be tested.

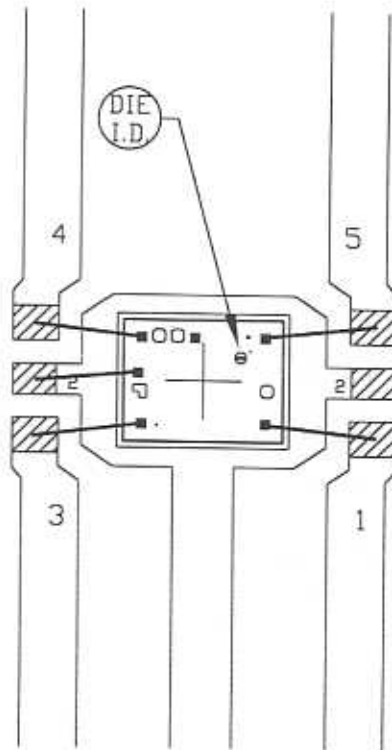
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





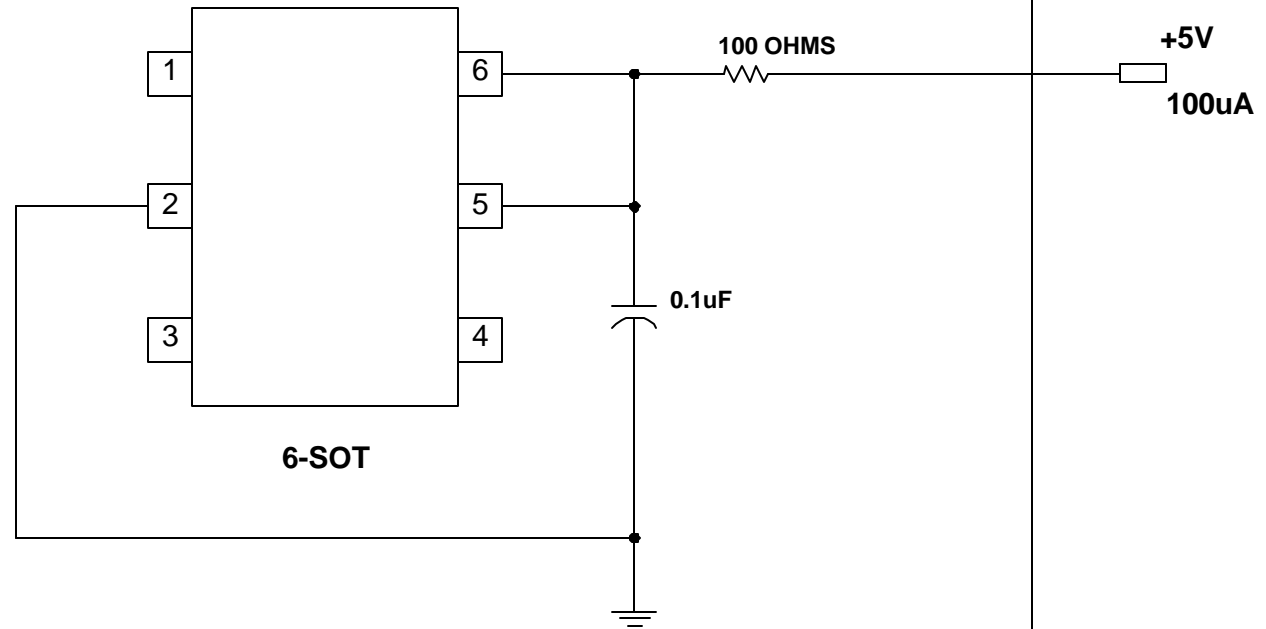
▨ - BONDING AREA

NOTE: CAVITY DOWN

PKG. CODE: U5-1		SIGNATURES	DATE	<b>MAXIM</b> CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 64X45	PKG. DESIGN			BOND DIAGRAM #: 05-1601-0124
				REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX6830

DRAWN BY: HAK TAN

MAX. EXPECTED CURRENT = 100uA

NOTES: