RELIABILITY REPORT

FOR

MAX6804USxxDx

PLASTIC ENCAPSULATED DEVICES

August 13, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6804 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6804 microprocessor (µP) supervisory circuit monitors the power supplies in 2.85V to 5.0V µP and digital systems. It increases circuit reliability and reduces cost by eliminating external components and adjustments. It also features a debounced manual reset input.

This devices performs a single function: it asserts a reset signal whenever the V_{CC} supply voltage declines below a preset threshold or whenever manual reset is asserted. Reset remains asserted for a preset timeout period after V_{CC} has risen above the reset threshold or after manual reset is deasserted. The MAX6804 (push/pull) has an active-low RESET-bar output. The MAX6804 is guaranteed to be in the correct state for V_{CC} down to 0.7V.

The reset comparator in this IC is designed to ignore fast transients on V_{CC}. Reset thresholds are factory-trimmable between 2.63V and 4.80V, in approximately 100mV increments. This device is available with a 1ms min, 20ms min, or 100ms min reset timeout period. Ideal for space-critical applications, the MAX6804 comes packaged in a 4-pin SOT143.

B. Absolute Maximum Ratings

Item	Rating
Terminal Voltage (with respect to GND)	
VCC	-0.3V to +6V
Push/Pull RESET or RESET , MR	-0.3V to (VCC + 0.3V)
Input Current (VCC)	20mA
Output Current (RESET, RESET)	20mA
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°
Terminal Voltage with Respect to GND	
Continuous Power Dissipation (TA = +70°C)	
4-Pin SOT143	320mW
Derates above +70°C	
4-Pin SOT143	4mW/°C

II. Manufacturing Information

A. Description/Function:	4-Pin, Low-Power µP Reset Circuits with Manual Reset
B. Process:	S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS
C. Number of Device Transistors:	505
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Thailand or Malaysia
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	**4 Lead SOT143**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0042
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	43 x 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec. # 06-4556) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS16-4 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MAX6804USxxDx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0
Moisture Testing				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	320	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic Package/Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

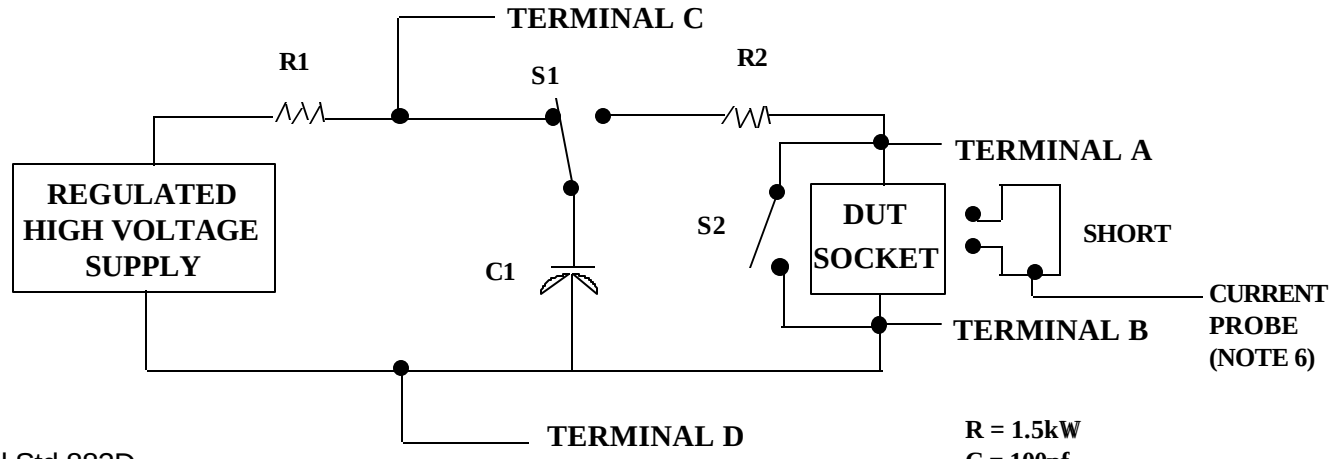
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

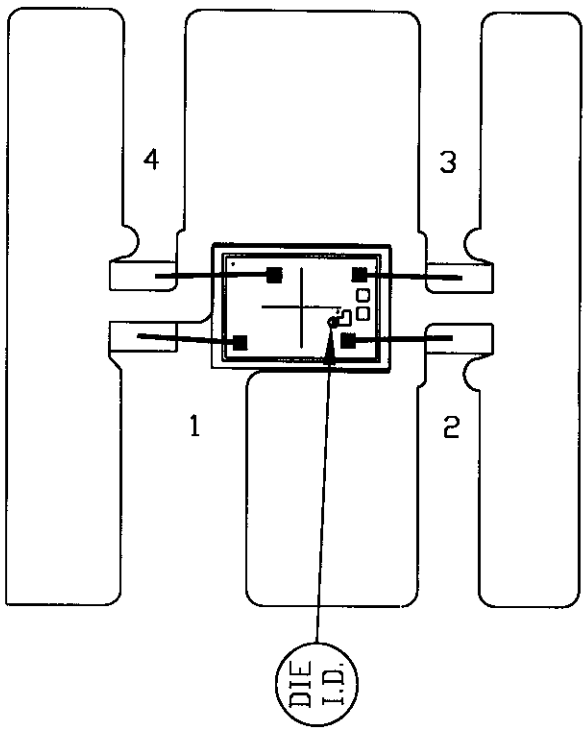
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



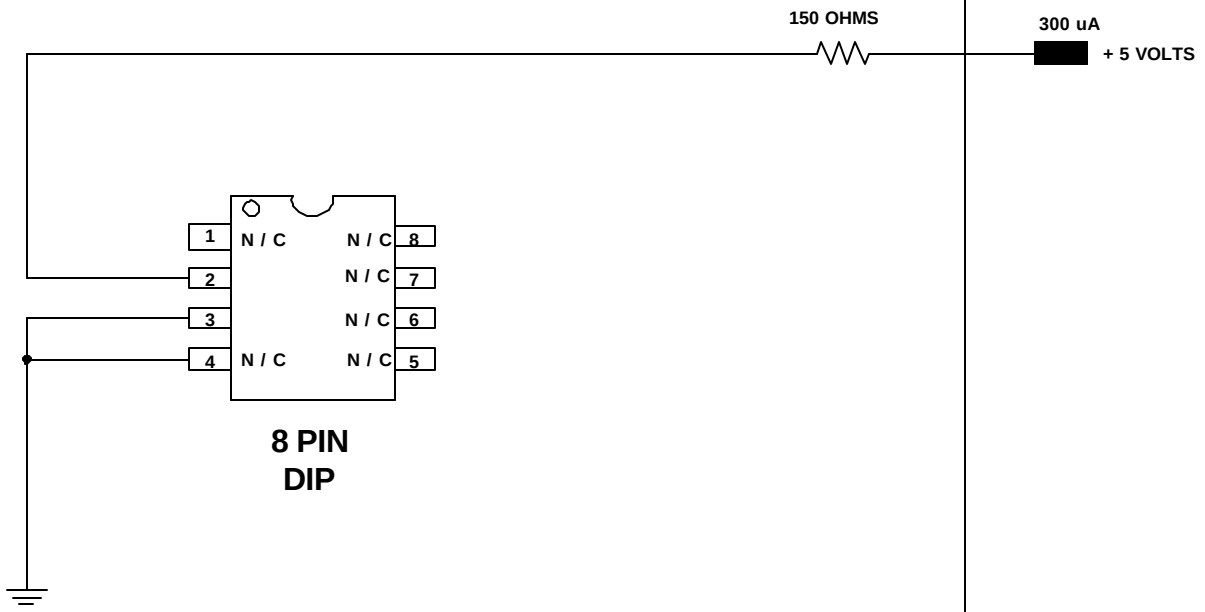
Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: U4-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 45X32	PKG. DESIGN			BUILDSHEET NUMBER: 05-1601-0042 / REV.: A

ONCE PER SOCKET

ONCE PER BOARD



8 PIN DIP

DEVICES: MAX 705/706/707/708/709/809/811/812/813/821/822/6314/6315/6326/6327/6328
MAX. EXPECTED CURRENT = 300 uA

DRAWN BY: TODD BEJSOVEC
NOTES: MS17 only for MAX 6326-28