MAX6690MEE
Rev. A

RELIABILITY REPORT

FOR

MAX6690MEE

PLASTIC ENCAPSULATED DEVICES

April 17, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX6690 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

The MAX6690 is a precise digital thermometer that reports the temperature of both a remote P-N junction and its own die. The remote junction can be a diode-connected transistor—typically a low-cost, easily mounted 2N3904 NPN type or 2N3906 PNP type—that replaces conventional thermistors or thermocouples. Remote accuracy is ±2°C for multiple transistor manufacturers, with no calibration needed. The remote junction can also be a common-collector PNP, such as a substrate PNP of a microprocessor (µP).

The 2-wire serial interface accepts standard System Management Bus (SMBus™), Write Byte, Read Byte, Send Byte, and Receive Byte commands to program the alarm thresholds and to read temperature data. Measurements can be done automatically and autonomously, with the conversion rate programmed by the user, or programmed to operate in a single-shot mode. The adjustable conversion rate allows the user to optimize supply current and temperature update rate to match system needs. When the conversion rate is faster than 1Hz, the conversion results are available as a 7-bit-plus-sign byte with a 1°C LSB. When the conversion rate is 1Hz or slower, the MAX6690 enters the extended mode. In this mode, 3 additional bits of temperature data are available in the extended resolution register, providing 10-bit-plus-sign resolution with a 0.125°C LSB. Single-shot conversions also have 0.125°C per LSB resolution when the conversion rate is 1Hz or slower.

A parasitic resistance cancellation (PRC) mode can also be invoked for conversion rates of 1Hz or slower by setting bit 4 of the configuration register to 1. In PRC mode, the effect of series resistance on the leads of the external diode is canceled. The 11-bit conversion in PRC mode is performed in <500ms and is disabled for conversion rates faster than 1Hz. The one-shot conversion is also 11 bits in <500ms.

The MAX6690 default low-temperature measurement limit is 0°C. This can be extended to -64°C by setting bit 5 of the configuration register to 1. The MAX6690 is available in a small, 16-pin QSOP surface-mount package.

B. Absolute Maximum Ratings

Item	Rating
(All voltages are referenced to GND unless otherwise noted.)	
VCC	-0.3V to +6V
DXP, ADD_	-0.3V to (VCC + 0.3V)
DXN	-0.3V to +0.8V
SMBCLK, SMBDATA, ALERT, STBY	-0.3V to +6V
SMBDATA, ALERT Current	-1mA to +50mA
DXN Current	±1mA
Operating Temperature Range	-55°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +165°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin QSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function: 2°C Accurate Remote/Local Temperature Sensor with SMBus Serial Interface

B. Process: S8

C. Number of Device Transistors: 12,504

D. Fabrication Location: California, USA

E. Assembly Location: Philippines, Malaysia or Thailand

F. Date of Initial Production: October, 2001

III. Packaging Information

A. Package Type: **16-Lead QSOP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-Filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-2901-0001

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 72 x 99 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliablity Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

(4389: Thermal acceleration factor assuming a 0.8eV activation energy)

$\lambda = 6.79 \times 10^{-9}$ λ= 6.79 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5592) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The TS04 die type has been found to have all pins able to withstand a transient pulse of 1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX6690MEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	160	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

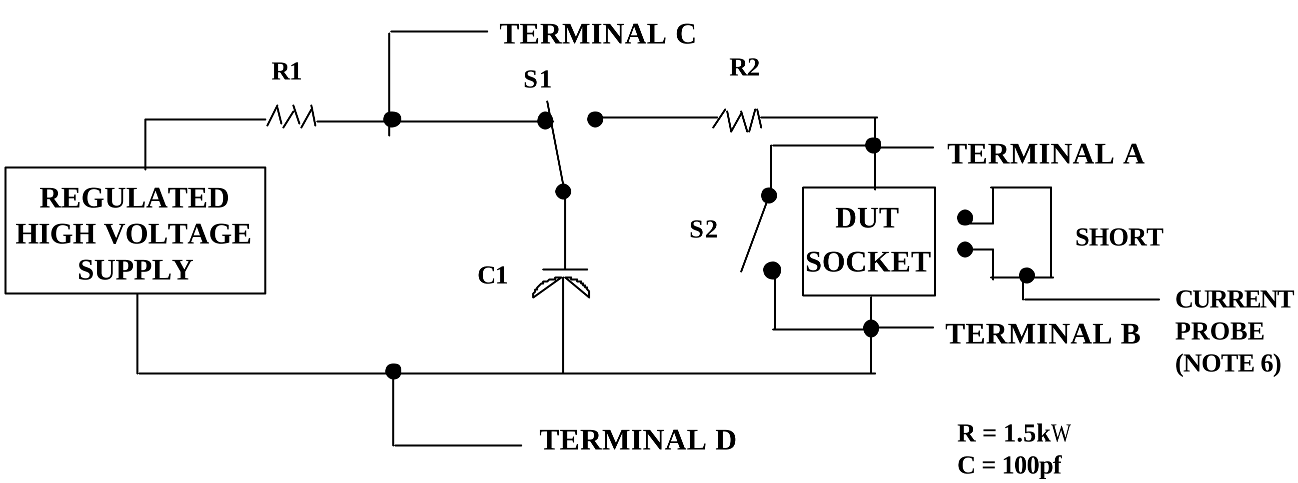
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

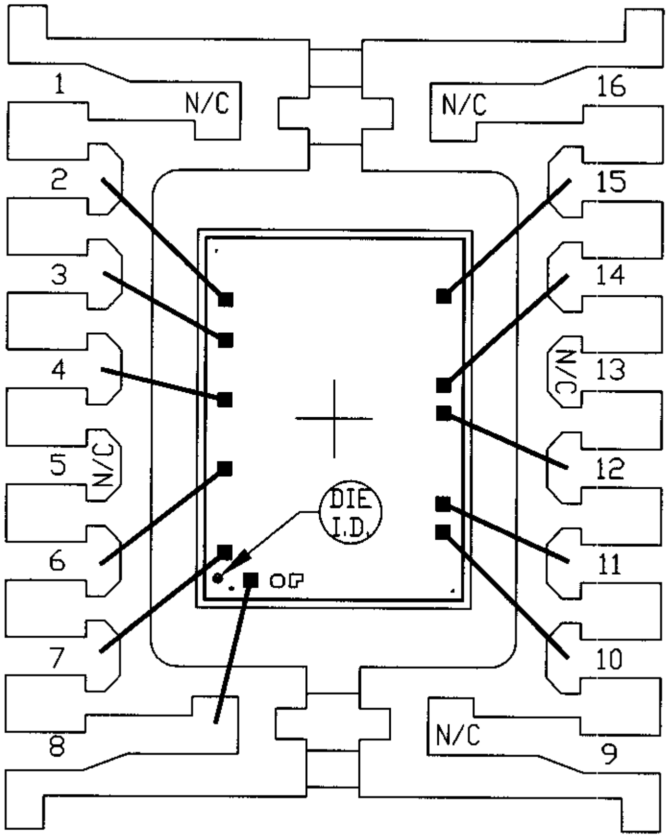
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

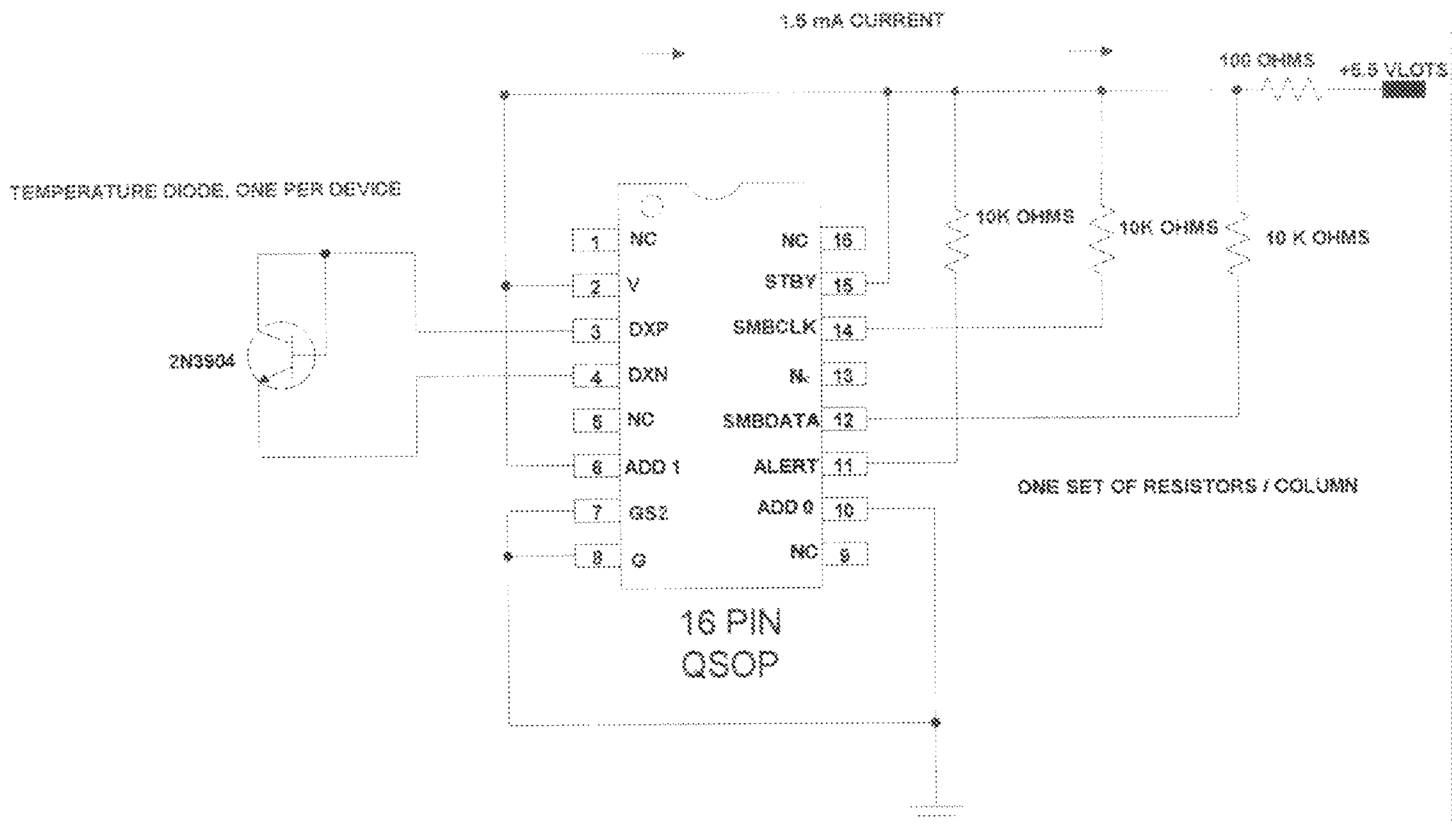




PKG. CODE: E16-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 96X130	PKG. DESIGN			BOND DIAGRAM #: 05-2901-0001	REV: A

ONCE PER SOCKET

ONCE PER BOARD



MAXIM BURN-IN SCHEMATIC SPEC 06-5592 REV. A DATE: 3 / 2 / 2000	DEVICES: MAX 6654 MAX. EXPECTED CURRENT = 1.5 mA	DRAWN BY: NOTES: